4-CHANNEL HD AUDIO CODEC WITH QUAD DIGITAL MICROPHONE INTERFACE

STAC9204/9205

Description

The STAC9204/9205 are high fidelity, 4-channel HD Audio CODECs that enable 2.0 Audio with simultaneous Real-Time Communication such as VoIP, conferencing, voice command and control, etc. Up to four digital microphones are supported, enabling high quality voice input for increased usability of voice applications.

Features

- High performance SD technology
  - 103dB DAC SNR
  - 90dB ADC SNR
- Two stereo DACs and two stereo ADCs
  - Supports 2.0 Audio with simultaneous Real-Time Communication (RTC) channel such as VoIP or separate stereo audio stream
  - Provides mono output for laptop sub-woofer
- 24-bit resolution with up to 192 KHz sample rates
- Supports advanced chipsets with flexible 1.5 V to 3.3 V signaling
- Digital microphone interface
  - Direct interface to up to four digital microphones
- Analog stereo microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
  - Five adjustable Vref outputs for microphone bias
- Universal Jacks™ functionality for jack retasking
- S/PDIF In and Out
- Two-pin volume up/down control
- Digital PC Beep to all outputs
- +3.3 V, +4 V, +4.5 V and +5 V analog power supply options
- Optimized and flexible power management
- 48-pin LQFP and 48-pad QFN environmental package

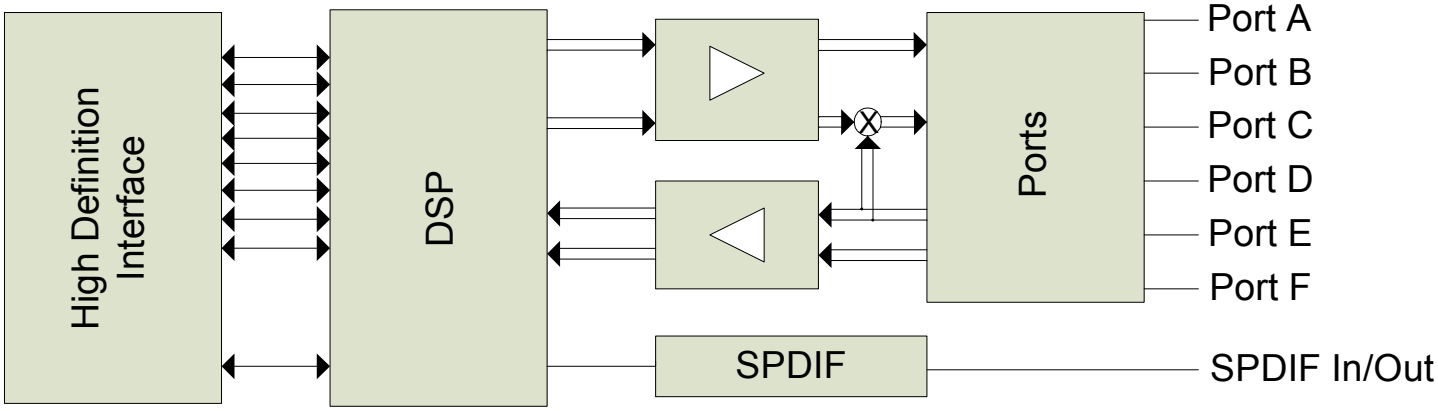
Software Support

- SKPI (Kernel Processing Interface)
  - Enables plug-ins that can operate globally on all audio streams of the system
- 12 band parametric equalizer SKPI plug-in
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing SKPI plug-in
  - Enables improved voice articulation
  - Compressor/limiter allows higher average noise level without resonances

Third Party Partners

- Dolby PC Entertainment Experience Logo Program
  - Dolby Home Theater™ (HT)
  - Dolby Sound Room™ (SR)
- Dolby Technologies
  - Dolby Headphone™, Dolby Virtual Speaker™
  - Dolby ProLogic II™, Dolby ProLogic IIx™
  - Dolby Digital Live™ (DDL)
- Intel Audio Studio™ from Sonic Focus
- Maxx Player™ from Waves
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression from Knowles™

Block Diagram



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1. DESCRIPTION

1.1. Overview

The STAC9204/9205 are high fidelity, 4-channel HD Audio CODECs that enable 2.0 Audio with simultaneous real-time communication such as VoIP, conferencing, voice command and control, etc. Up to four digital microphones are supported enabling high quality voice input for increased usability of voice applications.

The STAC9204/9205 incorporate IDT's proprietary SD technology to achieve a DAC SNR in excess of 100dB. The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9204/9205 provide stereo, 24-bit, full duplex resolution, supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9204/9205 SPDIF In/Out supports sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF OUT supports 88.2 KHz and 192 KHz. Additional sample rates are supported by the driver software.

The STAC9204/9205 support all desired four channel configurations, including switchable Headphone (HP) Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to consumer electronic equipment like Dolby Digital decoders, powered speakers and mini-disk drives, or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC. (Port D only supports fixed-function microphone.)

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9204/9205 have five General Purpose I/O (GPIO) pins. The STAC9204/9205 also provide single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9204/9205 integrate two headphone amplifiers which are available on Ports A and D. The headphone amplifiers are dedicated to these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected, and allow the CODECs to be reconfigured to support these devices regardless of which port they are connected to. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The STAC9204/9205 operate with a 3.3 V digital supply and either 3.3 V, 4 V, 4.5 V or 5 V analog supply. They also support 1.5 V and 3.3 V HDA signaling; the correct voltage is selected dynamically based on the value of the appropriate pin.

The STAC9204/9205 are available in a 48-pin LQFP or a 48-pad QFN Environmental (ROHS) package.

1.2. Block Diagram

Figure 1. STAC9204/9205 / STAC9204D/9205D Block Diagram

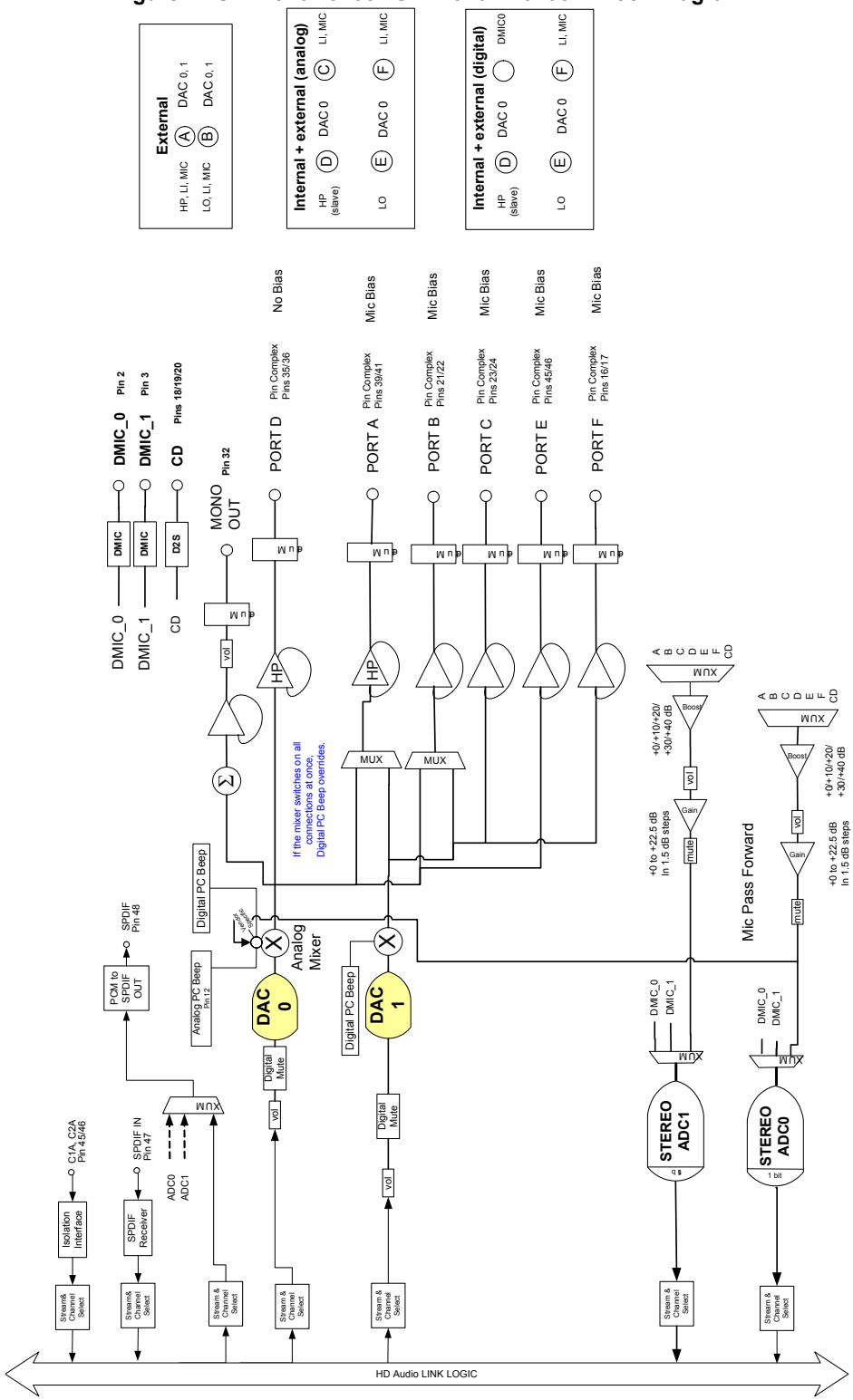
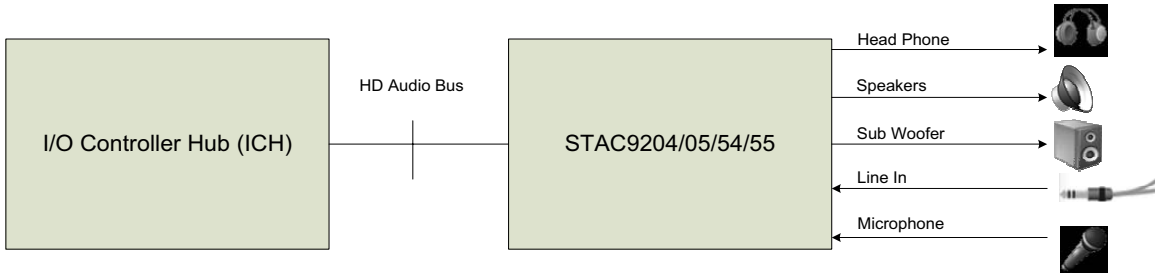


Figure 2. System Diagram



1.3. Detailed Description

1.3.1. Low-voltage High Definition Audio Link Signaling

The STAC9204/9205 are compatible with either 1.5 V or 3.3 V High Definition Audio Link signaling; the voltage selection is performed dynamically based on the input voltage of DVDD_IO. Note that DVDD_IO is not a logic configuration pin but provides the digital power supply to be used for the High Definition Audio Link signals.

When in 1.5 V mode, the STAC9204/9205 can correctly decode BITCLK, SYNC, RESET# and SDO because they operate at 1.5 V. Additionally, it will drive SDI_CODEC at 1.5 V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.3.2. Digital Microphone Support

The digital microphone interface permits connection of digital microphones to the STAC9205 via the DMIC0, DMIC1, and DMIC_CLK three-pin interface. The DMIC0 and DMIC1 pins carry either 1 or 2 channels of digital microphone data to the STAC9205. In the event that a single microphone is used, the data is routed to both ADC channels.

The DMIC_CLK output is programmable from 1.176 MHz to 4.704 MHz in 1.176 MHz increments and is synchronous to the 24 MHz internal clock. The default frequency is 2.352 MHz.

The STAC9205 supports the digital microphone configurations listed in Table 1.

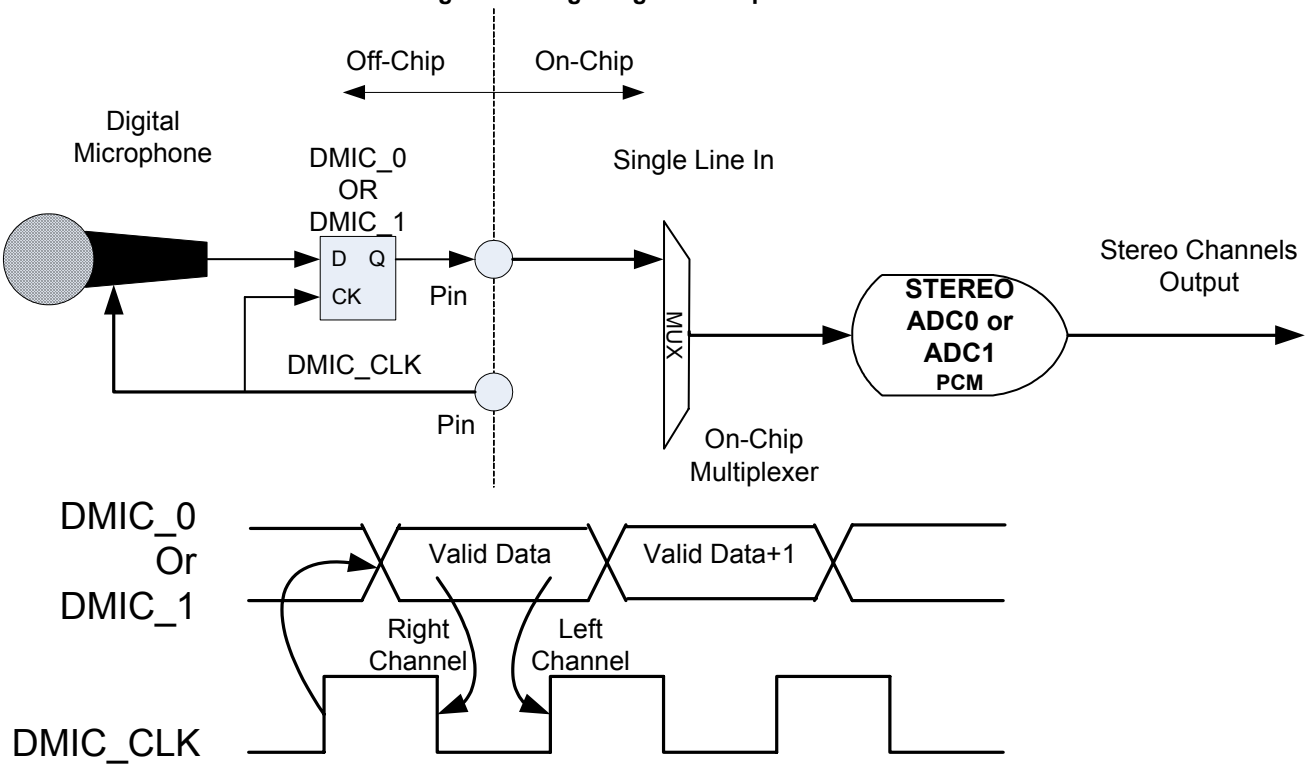
Table 1. STAC9205 Valid Digital Microphone Configurations

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge (see Figure 3)	0 or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels process data, may be in-phase or out-of-phase by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 (see Figure 4) *OR* Single Edge on DMIC_0 and 1	0 or 1	Available on either DMIC_0 or DMIC_1 External logic required to support sampling on a single Digital Microphone pin channel on rising edge and second Digital Microphone right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0 or 1	Requires both DMIC_0 or DMIC_1 External logic required to support sampling on a single Digital Microphone pin channel on rising edge and second Digital Microphone right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge (see Figure 5)	0 or 1	Connected to DMIC_0 and DMIC_1 External logic required to support sampling on a single Digital Microphone pin channel on rising edge and second Digital Microphone right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 2. DMIC_CLK, DMIC_0 and DMIC_1 Operation During Power States

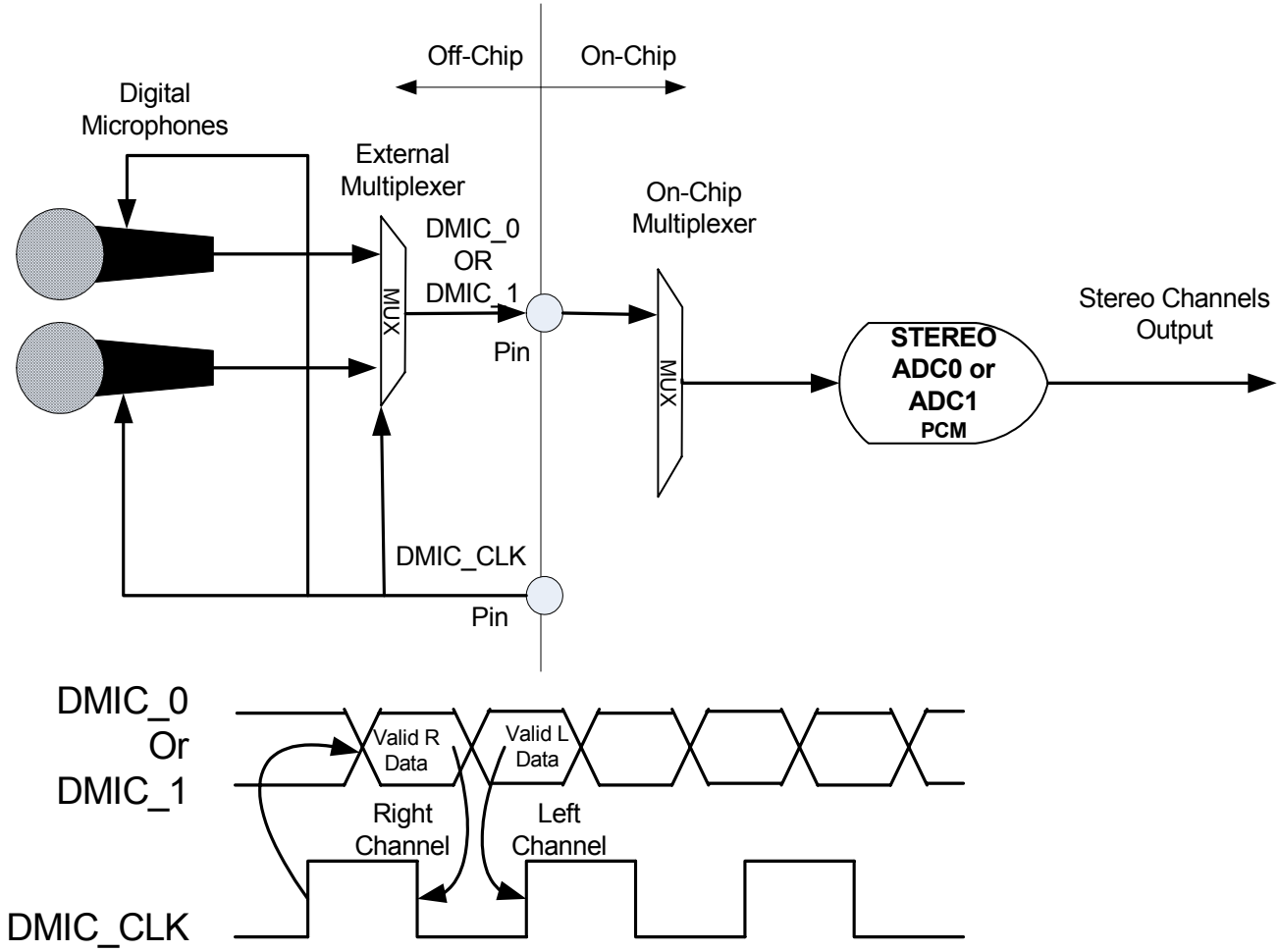
Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 input widget is enabled. Otherwise, the DMIC_CLK remains low.
D1	Yes	Clock Disabled	Input Disabled	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 input widget is enabled. Otherwise, the DMIC_CLK remains low.
D2	Yes	Clock Disabled	Input Disabled	DMIC_CLK remains low
D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK remains low
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with weak pull-down

Figure 3. Single Digital Microphone



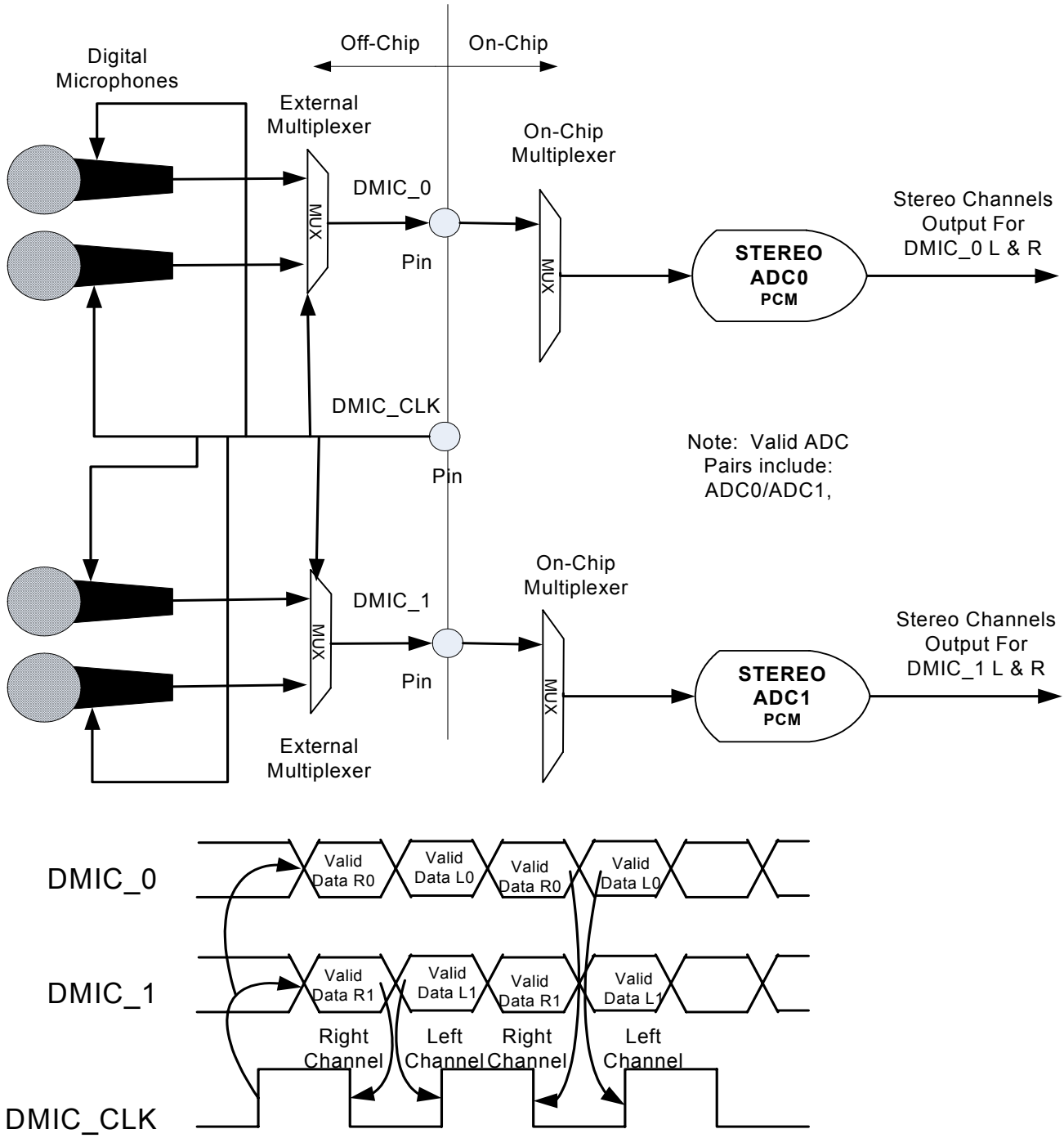
Note: Data is ported to both left and right channels.

Figure 4. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore the external mux may not be required.

Figure 5. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore the external mux may not be required

1.3.3. Volume/Digital Microphone/GPIO Selection

For the STAC9205, three functions are available on pins 2 and 3. To determine which function is actually enabled on these pins, the order of precedence is followed:

1. If the GPIOs are enabled through the Audio Function Group, they override both Volume Control and Digital Microphones.
2. If the GPIOs are not enabled through the Audio Function Group, then, at reset, the Volume control is enabled with a weak pull-up.
3. If BIOS or other software application enables either Digital Microphone input through the Configuration Default Register, the Volume is disconnected and the pull-ups are disconnected, with the weak pull-downs enabled.

For STAC9204, Digital Microphones are not available, but the other two functions operate with the same order of precedence.

1.3.4. VRefOut/GPIO Selection

Two functions are available on pins 30 and 31. To determine which function is enabled on the two pins, the order of precedence followed is:

1. If the GPIOs are enabled, they override VRefOut-E or VRefOut-F.
2. If the GPIOs are not activated through the Audio Function Group, then, at reset, the VRefOut pins are enabled.

If using the GPIOs as inputs, incorporate 10 KW external pull-ups or the GPI will not function correctly.

1.3.5. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz or 96 KHz, and implements internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record-slot-select and SPDIF_IN routing to the DAC allow for simultaneous record and play.

1.3.6. SPDIF Output

SPDIF Output supports 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz and 192 KHz sample rates, as defined in the Intel High Definition Audio Specification, with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

1.3.7. Mono Output

MONO Output is supported on pin 32 and has an independent mute and volume control. The MONO Output derives input from the output of the summing node after DAC0. The following analog signals feed the summing amplifier that feeds the MONO Output summing amplifier:

- DAC0 Output: When enabled, both DAC0 Outputs are summed together.
- Analog PC Beep: Sourced from pin 12.
- ADC Input: Stereo analog feed into the stereo ADC input.
- The combination of the stereo channels from DAC0 are combined into a single analog signal with a -6dB degradation in signal strength.

Note: MONO Output only works with the IDT Driver.

1.3.8. Universal Jacks™

The Universal Jacks™ technology allows for the greatest flexibility in board design and implementation.

For the STAC9204/9205 the Universal Jacks™ capabilities are as follows[1]:

- Ports A and D[2] support[3]:
  - Headphone Out
  - Line Out
  - Line In
  - Microphone, with 0/10/20/30/40 dB Microphone boost[4]
- Ports B, C, E, and F support[3]:
  - Line Out
  - Line In
  - Microphone, with 0/10/20/30/40 dB Microphone boost[4]
- Mono Output cannot be reconfigured

Note: 1) On the STAC9204/9205, only one function can be selected on each pin pair at a time. For example, a pin pair cannot be configured as an input and output at the same time. Configuration can be changed at any time.

Note: 2) Port D does not provide a microphone bias pin. Therefore only an internal, fixed-function microphone can be supported.

Note: 3) Headphone capabilities are provided on Ports A and D, however, audio performance degrades when 2 headphones are enabled.

Note: 4) When the 40dB microphone boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB microphone boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.3.8.1. Jack Detect

SENSE_A pin is used to detect the presence of plugs in ports A, B, C, and D. SENSE_B pin is used to detect the presence of plugs in ports E and F. Refer to the STAC9204/9205 reference design for port detect circuitry.

For different analog supply voltages, Table 3 summarizes what ports can be detected and the resistor tolerance needed.

Table 3. Jack Detect

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Sense A (If port D is used)	Resistor Tolerance Sense A (If port D is not used)	Resistor Tolerance Sense B (For ports E and F)
5 V	1%	1%	1%
4.5 V	1%	1%	1%
4 V	0.50%	1%	1%
3.3 V	0.10%	1%	1%

Includes pull-up resistors on Sense A/B and series resistors between jack switch and Sense A/B. See the reference design for more information on Jack Detect implementation.

1.3.8.2. Impedance Sense

Impedance Sensing is accomplished by on-chip circuitry that tests the impedance at the pin of the chip and compares it to internal reference impedance. Table 4 describes the bin information and the codes that are returned when the Pin Widget Impedance field in the Port Pin Sense widget is read. Please note that even under the best conditions, there is no method to guarantee 100% impedance sensing due to variations in external circuitry and impedance overlap of devices that can be plugged into a jack. The impedance sense table reflects both standard Line Out and Headphone output drivers.

Table 4. Impedance Sense

Bins	Return Hex Code	Measured Impedance Level	General Device Detected
000b	0064h	Impedance < 300 Ω	Passive Speakers, Headset Speakers
001b	012Ch	Impedance = 300 Ω +/- 25%	Some Headset Speakers
010b	028Ah	300 Ω > Impedance < 1275 Ω	Some Microphones
011b	03E8h	Impedance = 1275 Ω +/- 25%	Microphones
100b	07D0h	1275 Ω > Impedance < 2000 Ω	Microphones
101b	0BB8h	Impedance = 2000 Ω +/- 25%	Amplified Speakers
110b	2710h	> 2000 Ω	Amplified Speakers, Line In
111b	2710h	> 2000 Ω	Amplified Speakers, Line In

1.3.9. Power Management

Table 5 describes the active functionality in each power state.

Table 5. Power Management

Function	D0-D1	D2	D3-default	D3-alternate
DAC	On	Off	Off	Off
ADC	On	Off	Off	Off
Ports	On	On	Off	Off
Headphone (HP) Amps	On	On	Off[1]	Off
VrefOut	On	On	Off	Off
Port Sense	On	On	On[2]	Programmable
AZ-Link	On	On	On[3]	Programmable[4]
VAG	On	On	On[5]	Programmable
Differential Amplifiers	On	On	Off	Off

1. VAG is kept active when amplifiers are turned off.
2. If BITCLK is not active, a wake event must be generated. Otherwise an unsolicited response is sent.
3. Not active if BITCLK is not running.
4. This mode can only be exited with a Bus Reset.
5. VAG is always ramped up and down gradually, except in the case of a sudden power removal.

The D3-default state is available for HD Audio compliance. The programmable values exposed via vendor-specific settings are under the IDT Device Driver control for further power reduction.

The default power state for the Audio Function Group after reset is D3-default.

1.3.10. Analog PC-Beep

PC Beep may need to be active on power up, in which case the BIOS is responsible for enabling it by setting AnalogBeepEn in the AFG AnaCtrl widget. The PC_BEEP input is routed directly to the MONO_OUT, LINE_OUT and HP_OUT pins of the CODEC. Because the PC_BEEP input drive is often a full scale digital signal, some resistive attenuation of the PC_BEEP input is recommended to keep the beep tone within reasonable volume levels. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation.

Analog PC-Beep is not supported during Link Reset.

1.3.11. Headphone Drivers

Performance degradation will occur when using two headphones simultaneously. See the electrical specifications for details.

1.3.12. Device IDs

Table 6. Device IDs

Part Number	DAC SNR	DAC	ADC	Digital Mics	Dolby	VID	DID
STAC9205X	103dB	4	4	Yes	No	8384h	76A0h
STAC9205D	103dB	4	4	Yes	Yes-HT/SR	8384h	76A1h
STAC9204X	103dB	4	4	No	No	8384h	76A2h
STAC9204D	103dB	4	4	No	Yes-HT/SR	8384h	76A3h

Note: HT/SR refers to Dolby Home Theater (HT) and Sound Room (SR), logos of the Dolby PC Entertainment Experience Logo program.

2. CHARACTERISTICS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9204/9205. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{o}C to +70 ^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		Soldering temperature information for all available packages begins on page 189.

2.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: With Supply Override Enable Bit set to force 5 V operation.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 4.5 V	4.275	4.5	4.725	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C
	T_{case} (48-QFN)			+95	°C

ESD: The STAC9204/9205 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9204/9205 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.2. STAC9204/9205 5.0V, 4.5V, 4.0V, and 3.3V Analog Performance Characteristics

(Tambient = 25 ºC, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KW//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Table 7. Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Digital to Analog Converters						
Resolution		All		24		Bits
SNR - DAC to All Line-Out Ports (Note 4)	PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		103 101 100 98		dB
THD+N - DAC to All Line-Out Ports	-3dB Signal, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		87 85 84 82		dB
SNR - DAC to All Headphone Ports (Note 4)	10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		103 101 100 98		dB
THD+N - DAC to All Headphone Ports (Note 3)	-3dB Signal, 10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		85 83 82 80		dB
SNR - DAC to All Headphone Ports with 2 Headphone Outputs Operating (Note 4)	10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		100 98 97 95		dB
THD+N - DAC to All Headphone Ports with 2 Headphone Outputs Operating (Note 3)	-3dB Signal, 10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		82 80 79 77		dB
SNR - DAC to All Headphone Ports (Note 4)	32Ω load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		103 101 100 98		dB
THD+N - DAC to All Headphone Ports (Note 3)	-3dB Signal, 32Ω load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		80 80 78 76		dB
Any Analog Input to DAC Crosstalk	10KHz Signal Frequency	All	-	-80	-	dB
Any Analog Input to DAC Crosstalk	1KHz Signal Frequency	All	-	-85	-	dB
Gain Error	(Note 9)	All			0.5	dB
Interchannel Gain Mismatch	(Note 9)	All			0.5	dB

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Dynamic Range: PCM to All Analog Outputs (Note 1)	-60dB signal level	5V 4.5V 4.0V 3.3V	-	95 93 92 90	-	dB
D/A Digital Filter Pass Band (Note 5)		All	20	-	21,000	Hz
D/A Digital Filter Transition Band		All	21,000	-	31,000	Hz
D/A Digital Filter Stop Band		All	31,000	-	-	Hz
D/A Digital Filter Stop Band Rejection (Note 6)		All	-75	-	-	dB
D/A Out-of-Band Rejection (Notes 6 and 7)		All	-55	-	-	dB
Group Delay (48KHz sample rate)		All	-	-	1	ms
Attenuation, Gain Step Size DIGITAL		All	-	0.75	-	dB
Gain Drift		All	-	100	-	ppm/ºC
DAC Offset Voltage		All	-	20	100	mV
Deviation from Linear Phase		All	-	1	10	deg.
Analog Outputs						
Full Scale All Line-Outs	DAC PCM Data * (Note 11)	5V 4.5V 4.0V 3.3V	1.00 1.00 1.00 (*) 0.70	-	-	Vrms
Full Scale All Line-Outs	DAC PCM Data * (Note 11)	5V 4.5V 4.0V 3.3V	2.83 2.83 2.83 (*) 2.00	-	-	Vp-p
All Headphone Capable Outputs	32Ω load * (Note 11)	5V 4.5V 4.0V 3.3V	31 31 31 (*) 15	50 50 50 (*) 25	-	mWpeak
Analog inputs						
Full Scale Input Voltage	0dB Boost @4.75V	5V 4.5V 4.0V 3.3V	1.00	-	-	Vrms
All Analog Inputs with boost	10dB Boost	5V 4.5V 4.0V 3.3V	0.31	-	-	Vrms
All Analog Inputs with boost	20dB Boost	5V 4.5V 4.0V 3.3V	0.10	-	-	Vrms

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
All Analog Inputs with boost	30dB Boost	5V 4.5V 4.0V 3.3V	0.03	-	-	Vrms
All Analog Inputs with boost	40dB Boost (Not recommended)	5V 4.5V 4.0V 3.3V	0.01	-	-	Vrms
Input Impedance		All	-	50	-	KΩ
Input Capacitance		All	-	15	-	pF
Analog to Digital Converter						
Resolution		All		24		Bits
Dynamic Range, All Analog Inputs to A/D (Note 1)	High Pass Filer Enabled, 1Vrms Input, No boost	5V 4.5V 4.0V 3.3V	88	98 96 94 90		dB
SNR All Analog Inputs to A/D (Note 4)	High Pass Filter enabled, -3dBV input Level	5V 4.5V 4.0V 3.3V	88	98 96 94 90		dB
THD+N All Analog Inputs to A/D (Note 3)	High Pass Filter enabled, -3dBV input Level	5V 4.5V 4.0V 3.3V		85 80 74 72		dB
Analog Frequency Response (Note 2)		All	10	-	30,000	Hz
A/D Digital Filter Pass Band (Note 5)		All	20	-	21,000	Hz
A/D Digital Filter Transition Band		All	21,000	-	31,000	Hz
A/D Digital Filter Stop Band		All	31,000	-	-	Hz
A/D Digital Filter Stop Band Rejection (Note 6)		All	-90	-	-	dB
Group Delay (48KHz sample rate)		All	-	-	1	ms
Any Analog Input to ADC Crosstalk	10KHz Signal Frequency	All	-	-80	-	dB
Any Analog Input to ADC Crosstalk	1KHz Signal Frequency	All	-	-85	-	dB
Spurious Tone Rejection		All	-	-100	-	dB
Attenuation, Gain Step Size ANALOG		All	-	1.5	-	dB
Interchannel Gain Mismatch ADC		All	-	-	0.5	dB
Noise Floor when 40dB Mic Boost Enabled (40dB not recommended)		All			0.01	mV
40dB Mic Boost Enabled SNR (40dB not recommended)	5mV Input	All		60		dB

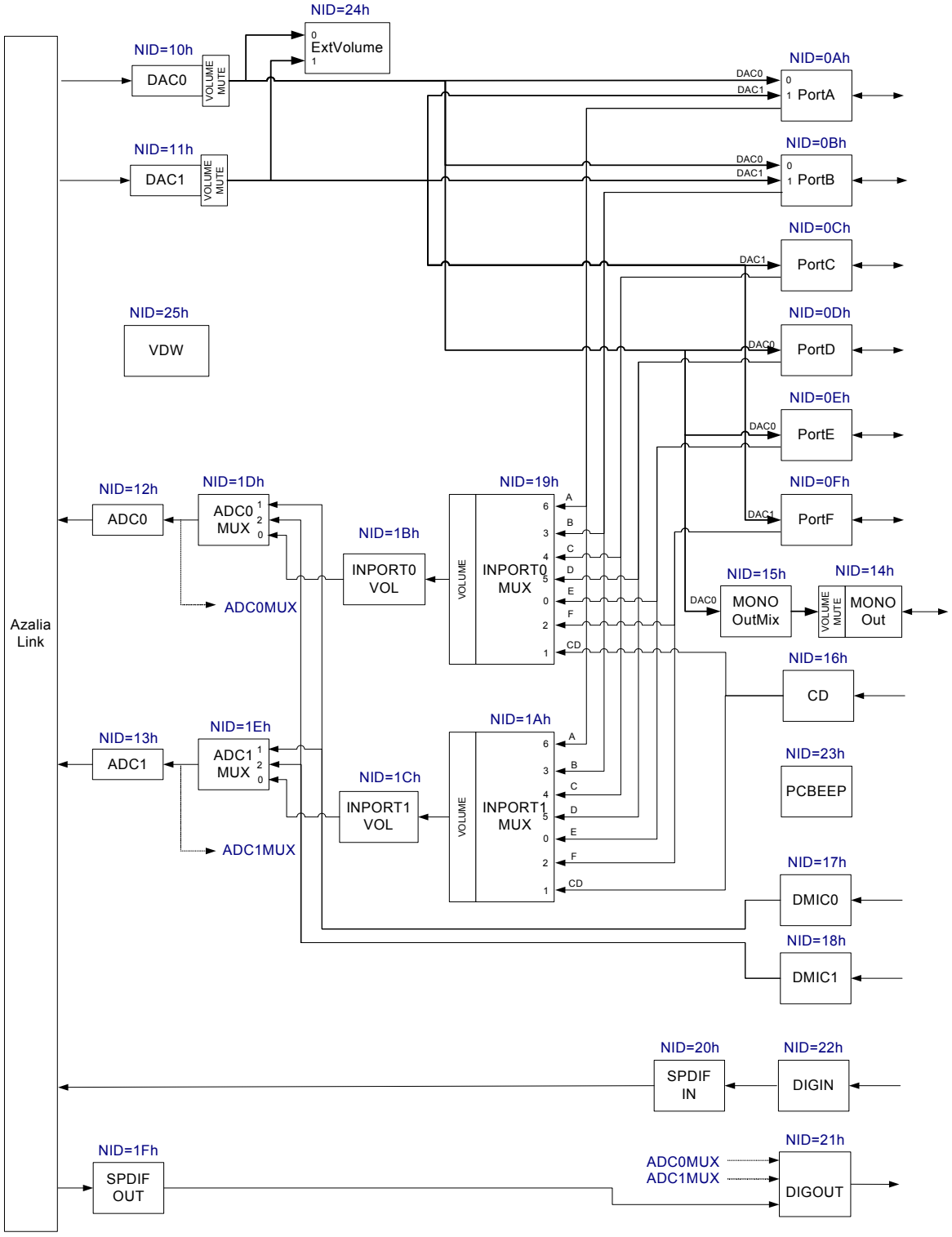
Parameter	Conditions	AVdd	Min	Typ	Max	Unit
40dB Mic Boost Enabled THD+N (40dB not recommended)	5mV Input	All		55		dB
Power Supply (Note 10)						
Power Supply Rejection Ratio	1kHz	All	-	-80	-	dB
Power Supply Rejection Ratio	20kHz	All	-	-70	-	dB
D0 Didd	3.3V			70	80	mA
D0 Aidd	5.0V 3.3V			65 50		mA
D1 Didd	3.3V			70	80	mA
D1 Aidd	5.0V 3.3V			65 50		mA
D2 Didd	3.3V			25	35	mA
D2 Aidd	5.0V 3.3V			43 35		mA
D3 Didd	3.3V			20	35	mA
D3 Aidd	5.0V 3.3V			20 17		mA
One Stereo ADC Didd	3.3V			3	5	mA
One Stereo ADC Aidd (note 12)	5.0V 3.3V			3	5	mA
One Stereo DAC Didd	3.3V			3	5	mA
One Stereo DAC Aidd (Note 12)	5.0V 3.3V			10	13	mA
CD Input						
CD Common Mode Rejection (CMR)		All	50	55		dB
Voltage Reference Outputs						
VREFout (Note 8)		All	-	0.5 X AVdd	-	V
VREFILT (VAG)		All		0.45X AVdd		V
Phased Locked Loop						
PLL lock time		All		96	200	usec
PLL (or HD Audio Bit CLK) 24MHz clock jitter		All		150	500	psec

1. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 kHz bandwidth.
2. ± 3dB limits for Line Output & 0 dB gain, at -20dBV
3. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 kHz bandwidth.
4. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
5. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 kHz Sample Frequency.
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.
8. Can be set to 0.5 or 0.8 AVdd.
9. Analog mixer disabled. See Figure 2
10. Didd= Didd_Core + Didd_IO (with all converters enabled and no playback)
11. Requires setting the power supply override bit.
12. Current reduction by disabling.

3. WIDGET INFORMATION AND SUPPORTED COMMAND VERBS

Figure 6. STAC9204/9205 Widget Diagram



3.1. Widget List STAC9204/9205

Table 8. High Definition Audio Widget

Node ID	Widget Name	Description
00h	Root	Root Node
01h	AFG	Audio Function Group
0Ah	Port A	Port A Pin Widget (Configurable as Headphone, Line In, Line Out, Microphone)
0Bh	Port B	Port B Pin Widget (Configurable as Line In, Line Out, Microphone)
0Ch	Port C	Port C Pin Widget (Configurable as Line In, Line Out, Microphone)
0Dh	Port D	Port D Pin Widget (Configurable as Headphone, Line In, Line Out, Microphone)
0Eh	Port E	Port E Pin Widget (Configurable as Line In, Line Out, Microphone)
0Fh	Port F	Port F Pin Widget (Configurable as Line In, Line Out, Microphone)
10h	DAC0	Stereo Output Converter to DAC
11h	DAC1	Stereo Output Converter to DAC
12h	ADC0	Stereo Input Converter to ADC
13h	ADC1	Stereo Input Converter to ADC
14h	Port MonoOut	Port MonoOut Pin Widget (output only)
15h	MonoOutMix	Port MonoOut Mixer
16h	CD	CD Pin Widget
17h	DigMic0	Digital Microphone 0 Pin Widget
18h	DigMic1	Digital Microphone 1 Pin Widget
19h	InPort0Mux	ADC0 Input Port Mux
1Ah	InPort1Mux	ADC1 Input Port Mux
1Bh	InPort0Vol	ADC0 Input Port Volume
1Ch	InPort1Vol	ADC1 Input Port Volume
1Dh	ADC0Mux	ADC0 Mux
1Eh	ADC1Mux	ADC1 Mux
1Fh	SPDIFOUT	Stereo Output for SPDIF_Out
20h	SPDIFIn	Stereo Input for SPDIF_In
21h	DigOut	Digital Output Pin
22h	DigIn	Digital Input Pin
23h	PcBeep	Digital PC Beep
24h	ExtVolume	External Volume Control
25h	Reserved	Reserved

3.2. Pin Configuration Default Register Settings

The configuration default registers are 32-bit registers required for each pin widget. These registers are normally used by the CODEC driver to determine the configuration of jacks and devices attached to the CODEC. When the CODEC is powered on, these registers are loaded with the default values provided by IDT for typical system usage, and are loaded in a way that is compatible with the Microsoft Universal Audio Architecture (UAA) driver. The values can be overridden by IDT customers according to their system configuration. Table 9 shows the Pin Widget Configuration Default settings.

Table 9. Pin Widget Configuration Default Settings

Pin Name	Port	Location	Device	Connection	Color	Misc	Assoc.	Seq
DigInPin	Not Connected 01b	Mainboard Rear 1h	SPDIF In Ch	RCA 4h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigOutPin	Connect to Jack 00b	Mainboard Rear 1h	SPDIF Out 4h	RCA 4h	Gray 2h	Jack Detect Override=0	7h	0h
PortAPin	Connect to Jack 00b	Mainboard Front 2h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	2h	0h
PortBPin	Connect to Jack 00b	Mainboard Front 2h	MIC In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	8h	0h
PortCPin	Connect to Jack 00b	Mainboard Rear 1h	Line In 8h	1/8 inch Jack 1h	Blue 3h	Jack Detect Override=0	4h	Eh
PortDPin	Connect to Jack 00b	Mainboard Rear 1h	HP Out 2h	1/8 inch Jack 1h	Green 4h	Jack Detect Override=0	1h	Fh
PortEPin	Connect to Jack 00b	Mainboard Rear 1h	Line Out 0h	1/8 inch Jack 1h	Black 1h	Jack Detect Override=0	1h	0h
PortFPin	Connect to Jack 00b	Mainboard Rear 1h	MIC In Ah	1/8 inch Jack 1h	Pink 9h	Jack Detect Override=0	4h	0h
MonoOutPin	Not Connected 01b	Internal 010000b	Line Out 0h	Other Analog 7h	Unknown 0h	Jack Detect Override=0	Fh	0h
CDPin	Not Connected 01b	Internal 010000b	CD 3h	ATAPI Internal 3h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic0Pin	Not Connected 01b	Internal 010000b	MIC In Ah	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h
DigMic1Pin	Not Connected 01b	Internal 010000b	MIC In Ah	Unknown 0h	Unknown 0h	Jack Detect Override=0	Fh	0h

3.3. Widget Information

Table 10. Command Format for Verb with 4-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:16]	BITS [15:0]
Reserved	CODEC Address	NID	Verb ID (4-bit)	Payload Data (16-bit)

Table 11. Command Format for Verb with 12-bit Identifier

Bits [39:32]	Bits [31:28]	BITS [27:20]	BITS[19:8]	BITS [7:0]
Reserved	CODEC Address	NID	Verb ID (12-bit)	Payload Data (8-bit)

There are two types of responses: Solicited and Unsolicited. Solicited responses are provided as a direct response to an issued command and will be provided in the frame immediately following the command. Unsolicited responses are provided by the CODEC independent of any command. Unsolicited responses are the result of CODEC events such as a jack insertion detection. The formats for Solicited Responses and Unsolicited Responses are shown in Tables 12 and 13 respectively. The “Tag” field in bits [31:28] of the Unsolicited Response identify the event.

Table 12. Solicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:0]
Valid (Valid = 1)	UnSol = 0	Reserved	Response

Table 13. Unsolicited Response Format

Bit [35]	Bit [34]	BITS [33:32]	BITS[31:28]	BITS [27:0]
Valid (Valid = 1)	UnSol = 1	Reserved	Tag	Response

3.4. Supported Command Verbs and Responses

3.4.1. Root Node (NID = 0x00)

3.4.1.1. Root PnpID

Table 14. Root PnpID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table.

Table 15. Root PnpID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID.
[15:8]	DeviceFix	R	0x76	Fixed portion of Device ID.
[7:0]	DeviceProg	R	0xA5	Dependant on device - See device ID table in section 1.3.12.

3.4.1.2. Root RevID

Table 16. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table.

Table 17. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant HD Audio spec.
[19:16]	Minor	R	0x0	Minor rev number of compliant HD Audio spec.
[15:12]	VendorFix	R	0x0	Vendor's rev number for this device.
[11:8]	VendorProg	R	0x1	Vendor's rev number for this device.

Table 17. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7:4]	SteppingFix	R	0x0	Vendor stepping number within the Vendor RevID.
[3:0]	SteppingProg	R	0x4	Vendor stepping number within the Vendor RevID.

3.4.1.3. Root NodeInfo

Table 18. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table.

Table 19. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

3.4.2. AFG Node (NID = 0x01)

3.4.2.1. AFG NodeInfo

Table 20. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table.

Table 21. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x0A	Starting node number for function group subordinate nodes.

Table 21. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x1C	Total number of nodes.

3.4.2.2. AFG Type

Table 22. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table.

Table 23. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:9]	Rsvd	R	0x0	Reserved
[8]	UnsolCap	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7:0]	NodeType	R	0x01	Node type = Audio Function Group

3.4.2.3. AFG GrpCap

Table 24. AFG GrpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table.

Table 25. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15:12]	Rsvd2	R	0x0	Reserved

Table 25. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[11:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.
[7:4]	Rsvd1	R	0x0	Reserved
[3:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

3.4.2.4. AFG FrmtCap

Table 26. AFG FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

Table 27. AFG FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported

Table 27. AFG FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) supported

3.4.2.5. AFG StreamCap

Table 28. AFG StreamCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

Table 29. AFG StreamCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x0	No support for non-PCM data.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

3.4.2.6. AFG InAmpCap

Table 30. AFG InAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0D	See bitfield table.

Table 31. AFG InAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x5	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x0F	Number of steps in the gain range = 15 (0dB to 22.5 dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

3.4.2.7. AFG PwrCap

Table 32. AFG PwrCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0F	See bitfield table.

Table 33. AFG PwrCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	D3	R	0x1	Power State D3 is supported. Allows for lowest possible power consuming state under software control (and still properly respond to a subsequent Power State command).
[2]	D2	R	0x1	Power State D2 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 ms.

Table 33. AFG PwrCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	D1	R	0x1	Power State D1 is supported. Allows for lowest possible power consuming state from which it can return to fully on state within 10 ms, excepting analog pass-through circuits which must remain fully on.
[0]	D0	R	0x1	Power State D0 is supported. Node power state is fully on.

3.4.2.8. AFG GPIOCap

Table 34. AFG GPIOCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	11	See bitfield table.

Table 35. AFG GPIOCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	GPIWake	R	0x1	Wake capability. Assuming the Wake Enable Mask controls are enabled, GPIOs configured as inputs can cause a wake (generate a Status Change event on the link) when there is a change in level on the pin.
[30]	GPIUnsol	R	0x1	Unsolicited Response capability. Assuming the Unsolicited Enable Mask controls are enabled, GPIOs configured as inputs can generate an Unsolicited Response on the link when there is a change in level on the pin.
[29:24]	Rsvd	R	0x0	Reserved
[23:16]	NumGPIs	R	0x00	Number of GPI pins supported by function
[15:8]	NumGPOs	R	0x00	Number of GPO pins supported by function
[7:0]	NumGPIOs	R	0x05	Number of GPIO pins supported by function

3.4.2.9. AFG OutAmpCap

Table 36. AFG OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 37. AFG OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x02	Size of each step in the gain range = 0.75dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x7F	Number of steps in the gain range = 128 (-95.25dB to +0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x7F	0dB-step is programmed with this offset

3.4.2.10. AFG PwrState

Table 38. AFG PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 39. AFG PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 39. AFG PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00: All Powered-On 01: D1 = > PR0, PR1 10: D2 = > PR0, PR1, PR2, PR6, EAPD 11: D3 = > PR6, PR5, PR3, PR2, PR1, PR0, EAPD Note: PR4 is not mapped in HD Audio

3.4.2.11. AFG UnsolResp

Table 40. AFG UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 41. AFG UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x0	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.2.12. AFG GPIO

Table 42. AFG GPIO Command Verb Format

	Verb ID	Payload	Response
Get	F15	00	See bitfield table.
Set1	715	See bits [7:0] of bitfield table.	0000_0000h

Table 43. AFG GPIO Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Data4	RW	0x0	Data for GPIO4. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[3]	Data3	RW	0x0	Data for GPIO3. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[2]	Data2	RW	0x0	Data for GPIO2. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[1]	Data1	RW	0x0	Data for GPIO1. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).
[0]	Data0	RW	0x0	Data for GPIO0. If this GPIO bit is configured as Sticky (edge-sensitive) input, it can be cleared by writing zero (one) here when the corresponding Polarity Control bit is zero (one).

3.4.2.13. AFG GPIOEn

Table 44. AFG GPIOEn Command Verb Format

	Verb ID	Payload	Response
Get	F16	00	See bitfield table.
Set1	716	See bits [7:0] of bitfield table.	0000_0000h

Table 45. AFG GPIOEn Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Mask4	RW	0x0	Enable for GPIO4: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[3]	Mask3	RW	0x0	Enable for GPIO3: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[2]	Mask2	RW	0x0	Enable for GPIO2: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[1]	Mask1	RW	0x0	Enable for GPIO1: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control
[0]	Mask0	RW	0x0	Enable for GPIO0: 0 = pin is disabled (Hi-Z state); 1 = pin is enabled; behavior determined by GPIO Direction control

3.4.2.14. AFG GPIODir

Table 46. AFG GPIODir Command Verb Format

	Verb ID	Payload	Response
Get	F17	00	See bitfield table.
Set1	717	See bits [7:0] of bitfield table.	0000_0000h

Table 47. AFG GPIODir Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Control4	RW	0x0	Direction control for GPIO4 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output

Table 47. AFG GPIODir Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	Control3	RW	0x0	Direction control for GPIO3 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[2]	Control2	RW	0x0	Direction control for GPIO2 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[1]	Control1	RW	0x0	Direction control for GPIO1 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output
[0]	Control0	RW	0x0	Direction control for GPIO0 0 = GPIO signal is configured as input 1 = GPIO signal is configured as output

3.4.2.15. AFG GPIOWake

Table 48. AFG GPIOWake Command Verb Format

	Verb ID	Payload	Response
Get	F18	00	See bitfield table.
Set1	718	See bits [7:0] of bitfield table.	0000_0000h

Table 49. AFG GPIOWake Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	En4	RW	0x0	Wake enable for GPIO4: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[3]	En3	RW	0x0	Wake enable for GPIO3: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.

Table 49. AFG GPIOWake Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	En2	RW	0x0	Wake enable for GPIO2: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[1]	En1	RW	0x0	Wake enable for GPIO1: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.
[0]	En0	RW	0x0	Wake enable for GPIO0: 0 = wake-up event is disabled; 1 = when HD Audio link is powered down (RST# is asserted), a wake-up event will trigger a Status Change Request event on the link.

3.4.2.16. AFG GPIOUnsol

Table 50. AFG GPIOUnsol Command Verb Format

	Verb ID	Payload	Response
Get	F19	00	See bitfield table.
Set1	719	See bits [7:0] of bitfield table.	0000_0000h

Table 51. AFG GPIOUnsol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	En4	RW	0x0	Unsolicited enable mask for GPIO4. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[3]	En3	RW	0x0	Unsolicited enable mask for GPIO3. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.

Table 51. AFG GPIOUnsol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	En2	RW	0x0	Unsolicited enable mask for GPIO2. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[1]	En1	RW	0x0	Unsolicited enable mask for GPIO1. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.
[0]	En0	RW	0x0	Unsolicited enable mask for GPIO0. If set, and the Unsolicited Response control for this widget has been enabled, an unsolicited response will be sent when GPIO0 is configured as input and changes state.

3.4.2.17. AFG GPIOSticky

Table 52. AFG GPIOSticky Command Verb Format

	Verb ID	Payload	Response
Get	F1A	00	See bitfield table.
Set1	71A	See bits [7:0] of bitfield table.	0000_0000h

Table 53. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	Mask4	RW	0x0	GPIO4 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

Table 53. AFG GPIOSticky Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	Mask3	RW	0x0	GPIO3 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[2]	Mask2	RW	0x0	GPIO2 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[1]	Mask1	RW	0x0	GPIO1 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.
[0]	Mask0	RW	0x0	GPIO0 input type (when configured as input): 0 = Non-Sticky (level-sensitive); 1 = Sticky (edge-sensitive). Sticky inputs are cleared by writing zero to corresponding bit of GPIO Data register. GPIOPolarity determines rising or falling edge sensitivity.

3.4.2.18. AFG SubID

Table 54. AFG SubID Command Verb Format

	Verb ID	Payload	Response
Get	F20	00	See bitfield table.
Set1	720	See bits [7:0] of bitfield table.	0000_0000h
Set2	721	See bits [7:0] of bitfield table.	0000_0000h

Table 54. AFG SubID Command Verb Format

	Verb ID	Payload	Response
Set3	722	See bits [7:0] of bitfield table.	0000_0000h
Set4	723	See bits [7:0] of bitfield table.	0000_0000h

Table 55. AFG SubID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Subsys3	RW	0x00	Subsystem ID. (Any non-zero value)
[23:16]	Subsys2	RW	0x00	Subsystem ID. (Any non-zero value)
[15:8]	Subsys1	RW	0x01	Subsystem ID. (Any non-zero value)
[7:0]	Assembly	RW	0x00	Assembly ID. (Not applicable to CODEC vendors)

3.4.2.19. AFG GPIOInvert

Table 56. AFG GPIOInvert Command Verb Format

	Verb ID	Payload	Response
Get	FEE	00	See bitfield table.
Set1	7EE	See bits [7:0] of bitfield table.	0000_0000h

Table 57. AFG GPIOInvert Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	GP4	RW	0x1	GPIO4 Polarity If configured as an output: 0 = inverting 1 = non-inverting If configured as a non-sticky input: 0 = inverting 1 = non-inverting If configured as a sticky input: 0 = falling events will be detected 1 = rising events will be detected.

Table 57. AFG GPIOInvert Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	GP3	RW	0x1	GPIO3 Polarity If configured as an output: 0 = inverting 1 = non-inverting If configured as a non-sticky input: 0 = inverting 1 = non-inverting If configured as a sticky input: 0 = falling events will be detected 1 = rising events will be detected.
[2]	GP2	RW	0x1	GPIO2 Polarity If configured as an output: 0 = inverting 1 = non-inverting If configured as a non-sticky input: 0 = inverting 1 = non-inverting If configured as a sticky input: 0 = falling events will be detected 1 = rising events will be detected.
[1]	GP1	RW	0x1	GPIO1 Polarity If configured as an output: 0 = inverting 1 = non-inverting If configured as a non-sticky input: 0 = inverting 1 = non-inverting If configured as a sticky input: 0 = falling events will be detected 1 = rising events will be detected.
[0]	GP0	RW	0x1	GPIO0 Polarity If configured as an output: 0 = inverting 1 = non-inverting If configured as a non-sticky input: 0 = inverting 1 = non-inverting If configured as a sticky input: 0 = falling events will be detected 1 = rising events will be detected.

3.4.2.20. AFG GPIODrive

Table 58. AFG GPIODrive Command Verb Format

	Verb ID	Payload	Response
Get	FEF	00	See bitfield table.
Set1	7EF	See bits [7:0] of bitfield table.	0000_0000h

Table 59. AFG GPIODrive Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:5]	Rsvd	R	0x0	Reserved
[4]	OD4	RW	0x0	GPIO4 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[3]	OD3	RW	0x0	GPIO3 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[2]	OD2	RW	0x0	GPIO2 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[1]	OD1	RW	0x0	GPIO1 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).
[0]	OD0	RW	0x0	GPIO0 Drive Mode; 0 = push-pull (drive 0 and 1), 1 = open drain (drive 0, float for 1).

3.4.2.21. AFG AnaCtrl

Table 60. AFG AnaCtrl Command Verb Format

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.
Set1	7E0	See bits [7:0] of bitfield table.	0000_0000h

Table 61. AFG AnaCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	AnaD3Enable	RW	0x0	D3 enable signal for analog
[6]	ADCMixDAC	RW	0x0	Enable mixing of ADC with DAC signal (for karaoke)
[5]	AnalogBeepEn	RW	0x0	Enable Analog PC-Beep path
[4]	LockLS	RW	0x0	Lock Level Shifters prior to digital power down while analog power still on (DEPENDS Bit) 0 = normal 1 = lock
[3]	UnlockLS	RW	0x0	Unlock Level Shifters 0 = lock 1 = Releases lock level shift.
[2]	Rsvd1	R	0x0	Reserved
[1:0]	VAGISel	RW	0x0	VAG amplifier output drive: 00 = nominal 01 = -50% 10 = +100% 11 = +50%

3.4.2.22. AFG Supply

Table 62. AFG Supply Command Verb Format

	Verb ID	Payload	Response
Get	FE6	00	See bitfield table.
Set1	7E6	See bits [7:0] of bitfield table.	0000_0000h

Table 63. AFG Supply Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd	R	0x0	Reserved
[7]	VAGRamp	RW	0x0	An internal power supply anti-pop circuit prevents audible clicks and pops from being heard when the CODEC is powered on and off. This function is accomplished by delaying the charge/discharge of the VREF capacitor. A value of C_{VREF} = 1 μF will cause a turn-on delay of roughly 3 seconds, which will allow the power supplies to stabilize before the CODEC outputs are enabled. The recommended value of C_{VREF} = 10 μF will extend the delay to 30 seconds. The CODEC outputs are also kept stable for the same amount of time at power-off to allow the system to be gracefully turned off. Setting the VAGRamp bit speeds up the ramp rate by 10X (degrading the anti-pop performance), for easier production testing. Any external component anti-pop circuit is unaffected by the internal circuit.
[6:5]	IBIAS	RW	0x0	00 = Normal Current 01 = 80% nominal Analog Current 10 = 120% nominal Analog Current 11 = 140% nominal Analog Current
[4]	SPDIFPinLvl	RW	0x1	0 = low-level SPDIF Input (special buffer for low level signals) 1 = standard SPDIF Input (for high level signals)
[3:0]	Override	RW	0x0	Supply Override Control. [0] = invert ADC supply [1] = invert DAC supply [2] = supply value [3] = supply override enable

3.4.2.23. AFG DMicCtrl

Table 64. AFG DMicCtrl Command Verb Format

	Verb ID	Payload	Response
Get	FF0	00	See bitfield table.
Set1	7F0	See bits [7:0] of bitfield table.	0000_0000h

Table 65. AFG DMicCtrl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3:2]	Phase	RW	0x0	Selects what phase of the DigMic clock the data should be latched: 0 = rising edge 1 = center of high 2 = falling edge 3 = center of low.
[1:0]	Rate	RW	0x2	Selects the DigMic rate: 0 = 4.704 MHz 1 = 3.528 MHz 2 = 2.352 MHz 3 = 1.176 MHz.

3.4.2.24. AFG Reset

Table 66. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table.
Set1	7FF	See bits [7:0] of bitfield table.	0000_0000h

Table 67. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

3.4.3. PortA Node (NID = 0x0A)

3.4.3.1. PortA WCap

Table 68. PortA WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 69. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported

Table 69. PortA WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.3.2. PortA PinCap

Table 70. PortA PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 71. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EAPDCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% AVdd; 50% AVdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.

Table 71. PortA PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

3.4.3.3. PortA ConnLen

Table 72. PortA ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 73. PortA ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x02	Number of NID entries in connection list. N = 02h if DAC1 enabled, N = 01h otherwise

3.4.3.4. PortA ConnLst

Table 74. PortA ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 75. PortA ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.

Table 75. PortA ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Entry1	R	0x11	DAC1 Converter widget. Entry1 = 11h if DAC1 enabled, Entry1 = 00h otherwise
[7:0]	Entry0	R	0x10	DAC0 Converter widget

3.4.3.5. PortA ConnSelect

Table 76. PortA ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 77. PortA ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:1]	Rsvd	R	0x0	Reserved
[0]	Index	RW	0x0	Connection select control index.

3.4.3.6. PortA PinCtl

Table 78. PortA PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 79. PortA PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HdphEn	RW	0x0	1 = enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled

Table 79. PortA PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VrefSelect	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z). (Hi-Z = 000b, 50% = 001b, GND = 010b, 80% = 100b)

3.4.3.7. PortA UnsolResp

Table 80. PortA UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 81. PortA UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.3.8. PortA PinSense

Table 82. PortA PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 83. PortA PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

3.4.3.9. PortA PinConfig

Table 84. PortA PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 85. PortA PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x02	Physical location of the jack. 02h = Mainboard, Front
[23:20]	Device	RW	0x2	Default Device, indicating intended use of jack. 2 = HP Out
[19:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15:12]	Color	RW	0x4	Color of physical jack. 4 = Green
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x2	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.4. PortB Node (NID = 0x0B)

3.4.4.1. PortB WCap

Table 86. PortB WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 87. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability

Table 87. PortB WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.4.2. PortB PinCap

Table 88. PortB PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 89. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin.
[15:8]	VrefCap	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% AVdd; 50% AVdd; GND; Hi-Z (required since pin complex is output capable)

Table 89. PortB PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphCap	R	0x0	Pin has a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement.
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

3.4.4.3. PortB ConnLen

Table 90. PortB ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 91. PortB ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x02	Number of NID entries in connection list. N = 02h if DAC1 enabled, N = 01h otherwise

3.4.4.4. PortB ConnLst

Table 92. PortB ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 93. PortB ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x11	DAC1 Converter widget. Entry1 = 11h if DAC1 enabled, Entry1 = 00h otherwise
[7:0]	Entry0	R	0x10	DAC0 Converter widget

3.4.4.5. PortB ConnSelect

Table 94. PortB ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 95. PortB ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:1]	Rsvd	R	0x0	Reserved
[0]	Index	RW	0x0	Connection select control index.

3.4.4.6. PortB PinCtl

Table 96. PortB PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 97. PortB PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VrefSelect	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z). (Hi-Z = 000b, 50% = 001b, GND = 010b, 80% = 100b)

3.4.4.7. PortB UnsolResp

Table 98. PortB UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 99. PortB UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.4.8. PortB PinSense

Table 100. PortB PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 101. PortB PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

3.4.4.9. PortB PinConfig

Table 102. PortB PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 103. PortB PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x02	Physical location of the jack. 02h = Mainboard, Front
[23:20]	Device	RW	0xA	Default Device, indicating intended use of jack. A = MIC In
[19:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15:12]	Color	RW	0x9	Color of physical jack. 9 = Pink
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x8	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.5. PortC Node (NID = 0x0C)

3.4.5.1. PortC WCap

Table 104. PortC WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 105. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability

Table 105. PortC WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present. ConnList = 1 if DAC1 enabled, ConnList = 0 otherwise
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.5.2. PortC PinCap

Table 106. PortC PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 107. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin

Table 107. PortC PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	VrefCap	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% AVdd; 50% AVdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable. OutCap = 1 if DAC1 enabled, OutCap = 0 otherwise
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

3.4.5.3. PortC ConnLen

Table 108. PortC ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 109. PortC ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list. N = 01h if DAC1 enabled, N = 00h otherwise

3.4.5.4. PortC ConnLst

Table 110. PortC ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 111. PortC ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x11	DAC1 Converter widget. Entry1 = 11h if DAC1 enabled, Entry1 = 00h otherwise

3.4.5.5. PortC PinCtl

Table 112. PortC PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 113. PortC PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled

Table 113. PortC PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VrefSelect	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z). (Hi-Z = 000b, 50% = 001b, GND = 010b, 80% = 100b)

3.4.5.6. PortC UnsolResp

Table 114. PortC UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 115. PortC UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.5.7. PortC PinSense

Table 116. PortC PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 117. PortC PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

3.4.5.8. PortC PinConfig

Table 118. PortC PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 119. PortC PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23:20]	Device	RW	0x8	Default Device, indicating intended use of jack. 8 = Line In
[19:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15:12]	Color	RW	0x3	Color of physical jack. 3 = Blue
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x4	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0xE	All Widgets in an association must have unique sequence number.

3.4.6. PortD Node (NID = 0x0D)

3.4.6.1. PortD WCap

Table 120. PortD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 121. PortD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability

Table 121. PortD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.6.2. PortD PinCap

Table 122. PortD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 123. PortD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.

Table 123. PortD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphCap	R	0x1	Pin complex has headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

3.4.6.3. PortD ConnLen

Table 124. PortD ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 125. PortD ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.6.4. PortD ConnLst

Table 126. PortD ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 127. PortD ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x10	DAC0 Converter widget

3.4.6.5. PortD PinCtl

Table 128. PortD PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 129. PortD PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HdphEn	RW	0x0	1 = enable the low impedance amplifier associated with the output.
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

3.4.6.6. PortD UnsolResp

Table 130. PortD UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 131. PortD UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.6.7. PortD PinSense

Table 132. PortD PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 133. PortD PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

3.4.6.8. PortD PinConfig

Table 134. PortD PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 135. PortD PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23:20]	Device	RW	0x2	Default Device, indicating intended use of jack. 2 = HP Out
[19:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15:12]	Color	RW	0x4	Color of physical jack. 4 = Green
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x1	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0xF	All Widgets in an association must have unique sequence number.

3.4.7. PortE Node (NID = 0x0E)

3.4.7.1. PortE WCap

Table 136. PortE WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 137. PortE WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.7.2. PortE PinCap

Table 138. PortE PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 139. PortE PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% AVdd; 50% AVdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

3.4.7.3. PortE ConnLen

Table 140. PortE ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 141. PortE ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.7.4. PortE ConnLst

Table 142. PortE ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 143. PortE ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x10	DAC0 Converter widget

3.4.7.5. PortE PinCtl

Table 144. PortE PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 145. PortE PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled

Table 145. PortE PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VrefSelect	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z). (Hi-Z = 000b, 50% = 001b, GND = 010b, 80% = 100b)

3.4.7.6. PortE UnsolResp

Table 146. PortE UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 147. PortE UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.7.7. PortE PinSense

Table 148. PortE PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 149. PortE PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

3.4.7.8. PortE PinConfig

Table 150. PortE PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 151. PortE PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23:20]	Device	RW	0x0	Default Device, indicating intended use of jack. 0 = Line Out
[19:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15:12]	Color	RW	0x1	Color of physical jack. 1 = Black
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x1	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.8. PortF Node (NID = 0x0F)

3.4.8.1. PortF WCap

Table 152. PortF WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 153. PortF WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability

Table 153. PortF WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present. ConnList = 1 if DAC1 enabled, ConnList = 0 otherwise
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.8.2. PortF PinCap

Table 154. PortF PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 155. PortF PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin

Table 155. PortF PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	VrefCap	R	0x17	VRef generation is supported by this pin complex, and the following voltages can be produced on the associated VRef pin: 80% AVdd; 50% AVdd; GND; Hi-Z (required since pin complex is output capable)
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x1	Pin complex is output capable. OutCap = 1 if DAC1 enabled, OutCap = 0 otherwise
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x1	Trigger is required for impedance measurement
[0]	ImpSenseCap	R	0x1	Pin complex supports impedance sense.

3.4.8.3. PortF ConnLen

Table 156. PortF ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 157. PortF ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list. N = 01h if DAC1 enabled, N = 00h otherwise

3.4.8.4. PortF ConnLst

Table 158. PortF ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 159. PortF ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x11	DAC1 Converter widget. Entry1 = 11h if DAC1 enabled, Entry1 = 00h otherwise

3.4.8.5. PortF PinCtl

Table 160. PortF PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 161. PortF PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled

Table 161. PortF PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[4:3]	Rsvd1	R	0x0	Reserved
[2:0]	VrefSelect	RW	0x0	VRefEn: Selects one of the possible states for the VRef signal associated with the Pin Widget. If the value written to this control does not correspond to a supported value defined in the VRefCntrl field of the Pin Capabilities parameter (0C), then this control will take the value of 000b (Hi-Z). (Hi-Z = 000b, 50% = 001b, GND = 010b, 80% = 100b)

3.4.8.6. PortF UnsolResp

Table 162. PortF UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 163. PortF UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.8.7. PortF PinSense

Table 164. PortF PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h
Set2	709	See bits [7:0] of bitfield table.	0000_0000h

Table 165. PortF PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	1 = something is plugged into jack associated with Pin Complex.
[30:0]	Impedance	R	0x7FFF_FFFF	Measured impedance of the widget. A value of all 1s indicates that a valid sense reading is not available, or the sense measurement is busy if it has been recently triggered.
[0]	RightCh	W	0x0	Set 1 = perform impedance sensing on right channel or ring of the connector
[0]	LeftCh	W	0x0	Set 0 = perform impedance sensing on left channel or tip of the connector

3.4.8.8. PortF PinConfig

Table 166. PortF PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 167. PortF PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23:20]	Device	RW	0xA	Default Device, indicating intended use of jack. A = MIC In
[19:16]	Connection	RW	0x1	Connection Type. 1 = 1/8 inch jack
[15:12]	Color	RW	0x9	Color of physical jack. 9 = Pink
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x4	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.9. DAC0 Node (NID = 0x10)

3.4.9.1. DAC0 CnvtrFrmt

Table 168. DAC0 CnvtrFrmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 169. DAC0 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.

Table 169. DAC0 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14]	RateBase	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	NumBits	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NumChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

3.4.9.2. DAC0 OutAmpRight

Table 170. DAC0 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 171. DAC0 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

3.4.9.3. DAC0 OutAmpLeft

Table 172. DAC0 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 173. DAC0 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

3.4.9.4. DAC0 WCap

Table 174. DAC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 175. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0xD	Number of sample delays through widget

Table 175. DAC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrPrsnt	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.9.5. DAC0 PwrState

Table 176. DAC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 177. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.

Table 177. DAC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

3.4.9.6. DAC0 CnvtrID

Table 178. DAC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 179. DAC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Stream	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Channel	RW	0x0	Integer representing lowest channel used by converter.

3.4.9.7. DAC0 LR

Table 180. DAC0 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 181. DAC0 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

3.4.10. DAC1 Node (NID = 0x11)

3.4.10.1. DAC1 CnvtrFrmt

Table 182. DAC1 CnvtrFrmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 183. DAC1 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	RateBase	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved

Table 183. DAC1 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	NumBits	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NumChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

3.4.10.2. DAC1 OutAmpRight

Table 184. DAC1 OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 185. DAC1 OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

3.4.10.3. DAC1 OutAmpLeft

Table 186. DAC1 OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 187. DAC1 OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Gain	RW	0x7F	Amplifier gain step number

3.4.10.4. DAC1 WCap

Table 188. DAC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 189. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Audio Output widget. Type = 0h (Output Converter) if DAC1 enabled, Type = Fh (Vendor Defined) otherwise
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrPrsnt	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present

Table 189. DAC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x1	Output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.10.5. DAC1 PwrState

Table 190. DAC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 191. DAC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down.

3.4.10.6. DAC1 CnvtrID

Table 192. DAC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 193. DAC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Stream	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Channel	RW	0x0	Integer representing lowest channel used by converter.

3.4.10.7. DAC1 LR

Table 194. DAC1 LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 195. DAC1 LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = enable swapping of left and right channels.
[1:0]	Rsvd1	R	0x0	Reserved

3.4.11. ADC0 Node (NID = 0x12)

3.4.11.1. ADC0 CnvtrFrmt

Table 196. ADC0 CnvtrFrmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 197. ADC0 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	RateBase	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 197. ADC0 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	NumBits	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NumChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

3.4.11.2. ADC0 WCap

Table 198. ADC0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 199. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrPrsnt	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x1	Software should query the Processing Controls parameter for this widget.

Table 199. ADC0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.11.3. ADC0 ConnLen

Table 200. ADC0 ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 201. ADC0 ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.11.4. ADC0 ConnLst

Table 202. ADC0 ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 203. ADC0 ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x1D	ADC0Mux widget

3.4.11.5. ADC0 ProcState

Table 204. ADC0 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.
Set1	703	See bits [7:0] of bitfield table.	0000_0000h

Table 205. ADC0 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

3.4.11.6. ADC0 PwrState

Table 206. ADC0 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 207. ADC0 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

3.4.11.7. ADC0 CnvtrID

Table 208. ADC0 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 209. ADC0 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Stream	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Channel	RW	0x0	Integer representing lowest channel used by converter

3.4.12. ADC1 Node (NID = 0x13)

3.4.12.1. ADC1 CnvtrFrmt

Table 210. ADC1 CnvtrFrmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 211. ADC1 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	R	0x0	Stream Type: only PCM streams are supported by this widget.
[14]	RateBase	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved

Table 211. ADC1 CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6:4]	NumBits	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NumChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

3.4.12.2. ADC1 WCap

Table 212. ADC1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 213. ADC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input
[19:16]	Delay	R	0xD	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right swap capability
[10]	PwrPrsnt	R	0x1	Power State control is supported
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x1	Software should query the Processing Controls parameter for this widget.

Table 213. ADC1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.12.3. ADC1 ConnLen

Table 214. ADC1 ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 215. ADC1 ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.12.4. ADC1 ConnLst

Table 216. ADC1 ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 217. ADC1 ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x1E	ADC1Mux widget

3.4.12.5. ADC1 ProcState

Table 218. ADC1 ProcState Command Verb Format

	Verb ID	Payload	Response
Get	F03	00	See bitfield table.
Set1	703	See bits [7:0] of bitfield table.	0000_0000h

Table 219. ADC1 ProcState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	HPFOCDIS	RW	0x0	High Pass Filter Offset Calculation Disable 0 = Calculation enabled. 1 = Calculation disabled.
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	ADCHPFByp	RW	0x1	Processing State = 00 (OFF): bypass the ADC high pass filter; Processing State = 01, 10, 11 (ON or BENIGN): ADC high pass filter is enabled.

3.4.12.6. ADC1 PwrState

Table 220. ADC1 PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 221. ADC1 PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - Fully on. 11 - Powered down (default)

3.4.12.7. ADC1 CnvtrID

Table 222. ADC1 CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 223. ADC1 CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Stream	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Channel	RW	0x0	Integer representing lowest channel used by converter

3.4.13. PortMonoOut Node (NID = 0x14)

3.4.13.1. PortMonoOut Vol

Table 224. PortMonoOut Vol Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 225. PortMonoOut Vol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:5]	Rsvd1	R	0x0	Reserved
[4:0]	Gain	RW	0x1F	Mono (left) amplifier gain step number

3.4.13.2. PortMonoOut WCap

Table 226. PortMonoOut WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 227. PortMonoOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream

Table 227. PortMonoOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x0	Mono widget

3.4.13.3. PortMonoOut PinCap

Table 228. PortMonoOut PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 229. PortMonoOut PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x00	VRef generation N/A since pin complex is not input capable.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.

Table 229. PortMonoOut PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

3.4.13.4. PortMonoOut OutAmpCap

Table 230. PortMonoOut OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 231. PortMonoOut OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x05	Size of each step in the gain range = 1.5dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x1F	Number of steps in the gain range = 31 (32 values, -46.5dB to +0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x1F	0dB-step is programmed with this offset

3.4.13.5. PortMonoOut ConnLen

Table 232. PortMonoOut ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 233. PortMonoOut ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.13.6. PortMonoOut ConnLst

Table 234. PortMonoOut ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 235. PortMonoOut ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x15	MonoOut Mix widget.

3.4.13.7. PortMonoOut PinCtl

Table 236. PortMonoOut PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 237. PortMonoOut PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved

Table 237. PortMonoOut PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5:0]	Rsvd1	R	0x0	Reserved

3.4.13.8. PortMonoOut PinConfig

Table 238. PortMonoOut PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 239. PortMonoOut PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x1	External Port Connectivity of the Pin Complex. 1 = no physical connection
[29:24]	Location	RW	0x10	Physical location of the jack. 10h = Internal, N/A
[23:20]	Device	RW	0x0	Default Device, indicating intended use of jack. 0 = Line Out
[19:16]	Connection	RW	0x7	Connection Type. 7 = Other Analog
[15:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0xF	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.14. MonoOutMix Node (NID = 0x15)

3.4.14.1. MonoOutMix WCap

Table 240. MonoOutMix WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 241. MonoOutMix WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x2	Widget type = Audio Mixer
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	Swapping of left and right channels not supported
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x0	Mono widget

3.4.14.2. MonoOutMix ConnLen

Table 242. MonoOutMix ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 243. MonoOutMix ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.14.3. MonoOutMix ConnLst

Table 244. MonoOutMix ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 245. MonoOutMix ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x10	DAC0 Converter widget

3.4.15. CD Node (NID = 0x16)

3.4.15.1. CD WCap

Table 246. CD WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 247. CD WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.15.2. CD PinCap

Table 248. CD PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 249. CD PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

3.4.15.3. CD PinCtl

Table 250. CD PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 251. CD PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

3.4.15.4. CD PinConfig

Table 252. CD PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 253. CD PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x1	External Port Connectivity of the Pin Complex. 1 = no physical connection
[29:24]	Location	RW	0x10	Physical location of the jack. 10h = Internal, N/A
[23:20]	Device	RW	0x3	Default Device, indicating intended use of jack. 3 = S887CD
[19:16]	Connection	RW	0x3	Connection Type. 3 = ATAPI internal
[15:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0xF	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.16. DigMic0 Node (NID = 0x17)

3.4.16.1. DigMic0 WCap

Table 254. DigMic0 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 255. DigMic0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Pin Complex widget. Type = 4h (Pin Complex) if DMIC enabled, Type = Fh (Vendor Defined) otherwise
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream (since the digital microphone input is a SDM signal that needs to be processed by the digital filters, it is not a true bit for bit digital stream like I^2S or SPDIF where samples are passed through unchanged)
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amplifier

Table 255. DigMic0 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.16.2. DigMic0 PinCap

Table 256. DigMic0 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 257. DigMic0 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

3.4.16.3. DigMic0 PinCtl

Table 258. DigMic0 PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 259. DigMic0 PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

3.4.16.4. DigMic0 PinConfig

Table 260. DigMic0 PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 261. DigMic0 PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x1	External Port Connectivity of the Pin Complex. 1 = no physical connection
[29:24]	Location	RW	0x10	Physical location of the jack. 10h = Internal, N/A
[23:20]	Device	RW	0xA	Default Device, indicating intended use of jack. A = MIC In
[19:16]	Connection	RW	0x0	Connection Type. 0 = Unknown

Table 261. DigMic0 PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0xF	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.17. DigMic1 Node (NID = 0x18)

3.4.17.1. DigMic1 WCap

Table 262. DigMic1 WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 263. DigMic1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Pin Complex widget. Type = 4h (Pin Complex) if DMIC enabled, Type = Fh (Vendor Defined) otherwise
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream (since the digital microphone input is a SDM signal that needs to be processed by the digital filters, it is not a true bit for bit digital stream like I^2S or SPDIF where samples are passed through unchanged)

Table 263. DigMic1 WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead.
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.17.2. DigMic1 PinCap

Table 264. DigMic1 PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 265. DigMic1 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x00	VRef generation not supported by this pin complex.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable.

Table 265. DigMic1 PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

3.4.17.3. DigMic1 PinCtl

Table 266. DigMic1 PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 267. DigMic1 PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

3.4.17.4. DigMic1 PinConfig

Table 268. DigMic1 PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 269. DigMic1 PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x1	External Port Connectivity of the Pin Complex. 1 = no physical connection
[29:24]	Location	RW	0x10	Physical location of the jack. 10h = Internal, N/A
[23:20]	Device	RW	0xA	Default Device, indicating intended use of jack. A = MIC In
[19:16]	Connection	RW	0x0	Connection Type. 0 = Unknown
[15:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0xF	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.18. InPort0Mux Node (NID = 0x19)

3.4.18.1. InPort0Mux WCap

Table 270. InPort0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 271. InPort0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability

Table 271. InPort0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.18.2. InPort0Mux OutAmpCap

Table 272. InPort0Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 273. InPort0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved

Table 273. InPort0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

3.4.18.3. InPort0Mux OutAmpRight

Table 274. InPort0Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 275. InPort0Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

3.4.18.4. InPort0Mux OutAmpLeft

Table 276. InPort0Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 277. InPort0Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB 001 = 10dB 010 = 20dB 011 = 30dB 100 = 40dB

3.4.18.5. InPort0Mux ConnSelect

Table 278. InPort0Mux ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 279. InPort0Mux ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

3.4.18.6. InPort0Mux ConnLen

Table 280. InPort0Mux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 281. InPort0Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x07	Number of NID entries in connection list.

3.4.18.7. InPort0Mux ConnLst

Table 282. InPort0Mux ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 283. InPort0Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x0B	Port B
[23:16]	Entry2	R	0x0F	Port F
[15:8]	Entry1	R	0x16	CD In
[7:0]	Entry0	R	0x0E	Port E

3.4.18.8. InPort0Mux ConnLst4

Table 284. InPort0Mux ConnLst4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 285. InPort0Mux ConnLst4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry7	R	0x0	No connection.
[23:16]	Entry6	R	0x0A	Port A
[15:8]	Entry5	R	0x0D	Port D
[7:0]	Entry4	R	0x0C	Port C

3.4.19. InPort1Mux Node (NID = 0x1A)

3.4.19.1. InPort1Mux WCap

Table 286. InPort1Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 287. InPort1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.19.2. InPort1Mux OutAmpCap

Table 288. InPort1Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 289. InPort1Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	No mute capability
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x27	Size of each step in the gain range = 10dB
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x04	Number of steps in the gain range = 5 (0dB to +40dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

3.4.19.3. InPort1Mux OutAmpRight

Table 290. InPort1Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 291. InPort1Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

3.4.19.4. InPort1Mux OutAmpLeft

Table 292. InPort1Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 293. InPort1Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd1	R	0x0	Reserved
[2:0]	Gain	RW	0x0	Amplifier gain step number: 000 = 0dB; 001 = 10dB; 010 = 20dB; 011 = 30dB; 100 = 40dB

3.4.19.5. InPort1Mux ConnSelect

Table 294. InPort1Mux ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 295. InPort1Mux ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2:0]	Index	RW	0x0	Connection select control index. (Default = Port E)

3.4.19.6. InPort1Mux ConnLen

Table 296. InPort1Mux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 297. InPort1Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x07	Number of NID entries in connection list.

3.4.19.7. InPort1Mux ConnLst

Table 298. InPort1Mux ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 299. InPort1Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x0B	Port B
[23:16]	Entry2	R	0x0F	Port F
[15:8]	Entry1	R	0x16	CD In
[7:0]	Entry0	R	0x0E	Port E

3.4.19.8. InPort1Mux ConnLst4

Table 300. InPort1Mux ConnLst4 Command Verb Format

	Verb ID	Payload	Response
Get	F02	04	See bitfield table.

Table 301. InPort1Mux ConnLst4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry7	R	0x0	No connection.
[23:16]	Entry6	R	0x0A	Port A

Table 301. InPort1Mux ConnLst4 Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Entry5	R	0x0D	Port D
[7:0]	Entry4	R	0x0C	Port C

3.4.20. InPort0Vol Node (NID = 0x1B)

3.4.20.1. InPort0Vol WCap

Table 302. InPort0Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 303. InPort0Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 303. InPort0Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x1	Input amplifier is present
[0]	Stereo	R	0x1	Stereo widget

3.4.20.2. InPort0Vol InAmpRight

Table 304. InPort0Vol InAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.
Set1	350	See bits [7:0] of bitfield table.	0000_0000h

Table 305. InPort0Vol InAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

3.4.20.3. InPort0Vol InAmpLeft

Table 306. InPort0Vol InAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.
Set1	360	See bits [7:0] of bitfield table.	0000_0000h

Table 307. InPort0Vol InAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

3.4.20.4. InPort0Vol ConnLen

Table 308. InPort0Vol ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 309. InPort0Vol ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.20.5. InPort0Vol ConnLst

Table 310. InPort0Vol ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

3.4.20.6.

Table 311. InPort0Vol ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	No Connection
[23:16]	Entry2	R	0x00	No Connection
[15:8]	Entry1	R	0x00	No Connection
[7:0]	Entry0	R	0x19	InPort0 Mux widget

3.4.21. InPort1Vol Node (NID = 0x1C)

3.4.21.1. InPort1Vol WCap

Table 312. InPort1Vol WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 313. InPort1Vol WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x1	Input amplifier is present
[0]	Stereo	R	0x1	Stereo widget

3.4.21.2. InPort1Vol InAmpRight

Table 314. InPort1Vol InAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B00	00	See bitfield table.
Set1	350	See bits [7:0] of bitfield table.	0000_0000h

Table 315. InPort1Vol InAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

3.4.21.3. InPort1Vol InAmpLeft

Table 316. InPort1Vol InAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	B20	00	See bitfield table.
Set1	360	See bits [7:0] of bitfield table.	0000_0000h

Table 317. InPort1Vol InAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd1	R	0x0	Reserved
[3:0]	Gain	RW	0x0	Amplifier gain step number

3.4.21.4. InPort1Vol ConnLen

Table 318. InPort1Vol ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 319. InPort1Vol ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.21.5. InPort1Vol ConnLst

Table 320. InPort1Vol ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 321. InPort1Vol ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	No Connection
[23:16]	Entry2	R	0x00	No Connection
[15:8]	Entry1	R	0x00	No Connection
[7:0]	Entry0	R	0x1A	InPort1Mux widget

3.4.22. ADC0Mux Node (NID = 0x1D)

3.4.22.1. ADC0Mux WCap

Table 322. ADC0Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 323. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector

Table 323. ADC0Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead
[3]	AmpOverride	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.22.2. ADC0Mux ConnSelect

Table 324. ADC0Mux ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 325. ADC0Mux ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

3.4.22.3. ADC0Mux ConnLen

Table 326. ADC0Mux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 327. ADC0Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x03	Number of NID entries in connection list. N = 03h if DMIC enabled, N = 01h otherwise

3.4.22.4. ADC0Mux ConnLst

Table 328. ADC0Mux ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 329. ADC0Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	No connection
[23:16]	Entry2	R	0x18	DMic1 Pin widget. Entry2 = 18h if DMIC enabled, Entry2 = 00h otherwise

Table 329. ADC0Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15:8]	Entry1	R	0x17	DMic0 Pin widget. Entry1 = 17h if DMIC enabled, Entry1 = 00h otherwise
[7:0]	Entry0	R	0x1B	InPort0Vol widget

3.4.22.5. ADC0Mux LR

Table 330. ADC0Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 331. ADC0Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = swap left and right channels of this Widget.
[1:0]	Rsvd1	R	0x0	Reserved

3.4.22.6. ADC0Mux OutAmpCap

Table 332. ADC0Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 333. ADC0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x00	Size of each step in the gain range, N/A since there are no steps

Table 333. ADC0Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x00	No steps, gain is fixed at 0dB
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

3.4.22.7. ADC0Mux OutAmpRight

Table 334. ADC0Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 335. ADC0Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

3.4.22.8. ADC0Mux OutAmpLeft

Table 336. ADC0Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 337. ADC0Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved

Table 337. ADC0Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

3.4.23. ADC1Mux Node (NID = 0x1E)

3.4.23.1. ADC1Mux WCap

Table 338. ADC1Mux WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 339. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x3	Widget type = Audio Selector
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x1	Left and right channels can be swapped
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x0	Widget supports an Analog stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter.
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	No format info; use default format parameters from Audio Function node instead

Table 339. ADC1Mux WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[3]	AmpOverride	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.23.2. ADC1Mux ConnSelect

Table 340. ADC1Mux ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 341. ADC1Mux ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

3.4.23.3. ADC1Mux ConnLen

Table 342. ADC1Mux ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 343. ADC1Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved

Table 343. ADC1Mux ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x03	Number of NID entries in connection list. N = 03h if DMIC enabled, N = 01h otherwise

3.4.23.4. ADC1Mux ConnLst

Table 344. ADC1Mux ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 345. ADC1Mux ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	No connection
[23:16]	Entry2	R	0x18	DMic1 Pin widget. Entry2 = 18h if DMIC enabled, Entry2 = 00h otherwise
[15:8]	Entry1	R	0x17	DMic0 Pin widget. Entry1 = 17h if DMIC enabled, Entry1 = 00h otherwise
[7:0]	Entry0	R	0x1C	InPort1Vol widget

3.4.23.5. ADC1Mux LR

Table 346. ADC1Mux LR Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 347. ADC1Mux LR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd2	R	0x0	Reserved
[2]	SwapEn	RW	0x0	1 = swap left and right channels of this Widget.
[1:0]	Rsvd1	R	0x0	Reserved

3.4.23.6. ADC1Mux OutAmpCap

Table 348. ADC1Mux OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 349. ADC1Mux OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x1	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x00	Size of each step in the gain range, N/A since there are no steps
[15]	Rsvd2	R	0x0	Reserved
[14:8]	NumSteps	R	0x00	No steps, gain is fixed at 0dB
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x00	0dB-step is programmed with this offset

3.4.23.7. ADC1Mux OutAmpRight

Table 350. ADC1Mux OutAmpRight Command Verb Format

	Verb ID	Payload	Response
Get	B80	00	See bitfield table.
Set1	390	See bits [7:0] of bitfield table.	0000_0000h

Table 351. ADC1Mux OutAmpRight Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

3.4.23.8. ADC1Mux OutAmpLeft

Table 352. ADC1Mux OutAmpLeft Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 353. ADC1Mux OutAmpLeft Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x1	1 = mute is active
[6:0]	Rsvd1	R	0x0	Reserved

3.4.24. SPDIFOut Node (NID = 0x1F)

3.4.24.1. SPDIFOut CnvtrFrmt

Table 354. SPDIFOut CnvtrFrmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 355. SPDIFOut CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)
[14]	RateBase	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	NumBits	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NumChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

3.4.24.2. SPDIFOut WCap

Table 356. SPDIFOut WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 357. SPDIFOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x0	Widget type = Audio Output
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x1	Widget contains format info; software should query
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.24.3. SPDIFOut FrmtCap

Table 358. SPDIFOut FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

Table 359. SPDIFOut FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x0	176.4 KHz rate (4/1*44.1 KHz) NOT supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

3.4.24.4. SPDIFOut StreamCap

Table 360. SPDIFOut StreamCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

Table 361. SPDIFOut StreamCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

3.4.24.5. SPDIFOut CnvtrID

Table 362. SPDIFOut CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 363. SPDIFOut CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Stream	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Channel	RW	0x0	Integer representing lowest channel used by converter

3.4.24.6. SPDIFOut DigCtl

Table 364. SPDIFOut DigCtl Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.
Set1	70D	See bits [7:0] of bitfield table.	0000_0000h
Set2	70E	See bits [7:0] of bitfield table.	0000_0000h

Table 365. SPDIFOut DigCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	Rsvd1	R	0x0	Rsvd
[14:8]	CC	RW	0x00	CC[6:0] - Category Code
[7]	L	RW	0x0	L - Generation Level
[6]	PRO	RW	0x0	PRO - Professional
[5]	AUDIO	RW	0x0	/AUDIO - Non-Audio
[4]	COPY	RW	0x0	COPY - Copyright
[3]	PRE	RW	0x0	PRE - Pre-emphasis
[2]	VCFG	RW	0x0	VCFG - Validity Config
[1]	V	RW	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

3.4.25. SPDIFIn Node (NID = 0x20)

3.4.25.1. SPDIFIn CnvtrFrmt

Table 366. SPDIFIn CnvtrFrmt Command Verb Format

	Verb ID	Payload	Response
Get	A	0000	See bitfield table.
Set1	2	See bits [15:0] of bitfield table.	0000_0000h

Table 367. SPDIFIn CnvtrFrmt Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Rsvd2	R	0x0	Reserved
[15]	StrmType	RW	0x0	Stream Type 0 = PCM 1 = Non-PCM (remaining bits in this verb have other meanings)
[14]	RateBase	RW	0x0	Sample Base Rate 0 = 48 KHz 1 = 44.1 KHz
[13:11]	RateMult	RW	0x0	Sample Base Rate Multiple 000 = 48 KHz / 44.1 KHz or less 001 = x2 010 = Reserved (x3) 011 = x4 100-111 = Reserved
[10:8]	RateDiv	RW	0x0	Sample Base Rate Divisor 000 = Divide by 1 001 = Divide by 2 010 = Divide by 3 011 = Divide by 4 100 = Divide by 5 101 = Divide by 6 110 = Divide by 7 111 = Divide by 8
[7]	Rsvd1	R	0x0	Reserved
[6:4]	NumBits	RW	0x3	Bits per Sample 000 = 8 bits 001 = 16 bits 010 = 20 bits 011 = 24 bits 100-111 = Reserved
[3:0]	NumChan	RW	0x1	Number of Channels Number of channels in each frame of the stream. 0000 = 1 channel 0001 = 2 channels ... 1111 = 16 channels

3.4.25.2. SPDIFIn WCap

Table 368. SPDIFIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 369. SPDIFIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x1	Widget type = Audio Input. Input Converter (1h) if SPDIFIn enabled, Vendor Defined (Fh) otherwise
[19:16]	Delay	R	0x4	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	Unsolicited Response is not supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x1	Widget contains format info; software should query
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.25.3. SPDIFIn FrmtCap

Table 370. SPDIFIn FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table.

Table 371. SPDIFIn FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x0	192.0 KHz rate (4/1*48 KHz) NOT supported
[9]	R10	R	0x0	176.4 KHz rate (4/1*44.1 KHz) NOT supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x0	88.2 KHz rate (2/1*44.1 KHz) NOT supported
[6]	R7	R	0x1	48.0 KHz rate supported (REQUIRED)
[5]	R6	R	0x1	44.1 KHz rate supported
[4]	R5	R	0x0	32.0 KHz rate (2/3*48 KHz) NOT supported
[3]	R4	R	0x0	22.05 KHz rate (1/2*44.1 KHz) NOT supported
[2]	R3	R	0x0	16.0 KHz rate (1/3*48 KHz) NOT supported
[1]	R2	R	0x0	11.025 KHz rate (1/4*44.0 KHz) NOT supported
[0]	R1	R	0x0	8.0 KHz rate (1/6*48 KHz) NOT supported

3.4.25.4. SPDIFIn StreamCap

Table 372. SPDIFIn StreamCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0B	See bitfield table.

Table 373. SPDIFIn StreamCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:3]	Rsvd	R	0x0	Reserved
[2]	NonPCM	R	0x1	Non-PCM data supported.
[1]	Float32	R	0x0	No support for Float32 data.
[0]	PCM	R	0x1	PCM-formatted data supported.

3.4.25.5. SPDIFIn ConnLen

Table 374. SPDIFIn ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 375. SPDIFIn ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x01	Number of NID entries in connection list.

3.4.25.6. SPDIFIn ConnLst

Table 376. SPDIFIn ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 377. SPDIFIn ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	Unused list entry.
[23:16]	Entry2	R	0x00	Unused list entry.
[15:8]	Entry1	R	0x00	Unused list entry.
[7:0]	Entry0	R	0x22	DigIn pin widget

3.4.25.7. SPDIFIn CnvtrID

Table 378. SPDIFIn CnvtrID Command Verb Format

	Verb ID	Payload	Response
Get	F06	00	See bitfield table.
Set1	706	See bits [7:0] of bitfield table.	0000_0000h

Table 379. SPDIFIn CnvtrID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:4]	Stream	RW	0x0	Software-programmable integer representing link stream ID used by the converter widget. By convention, stream 0 is reserved as unused.
[3:0]	Channel	RW	0x0	Integer representing lowest channel used by converter

3.4.25.8. SPDIFIn DigCtl

Table 380. SPDIFIn DigCtl Command Verb Format

	Verb ID	Payload	Response
Get	F0D	00	See bitfield table.
Set1	70D	See bits [7:0] of bitfield table.	0000_0000h
Set2	70E	See bits [7:0] of bitfield table.	0000_0000h

Table 381. SPDIFIn DigCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:15]	Rsvd2	R	0x0	Reserved
[14:8]	CC	R	0x00	CC[6:0] - Category Code
[7]	L	R	0x0	L - Generation Level
[6]	PRO	R	0x0	PRO - Professional
[5]	AUDIO	R	0x0	/AUDIO - Non-Audio
[4]	COPY	R	0x0	COPY - Copyright
[3]	PRE	R	0x0	PRE - Pre-emphasis
[2]	Rsvd1	R	0x0	Reserved (VCFG bit applies only to output streams)
[1]	V	R	0x0	V - Validity
[0]	DigEn	RW	0x0	DigEn - Digital Enable

3.4.25.9. SPDIFIn VSR

Table 382. SPDIFIn VSR Command Verb Format

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.
Set1	7E0	See bits [7:0] of bitfield table.	0000_0000h

Table 383. SPDIFIn VSR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	RcvRateBase	R	0x0	Recovered sample rate base 0 = 48 KHz 1 = 44.1 KHz
[30:28]	RcvRateMult	R	0x0	Recovered sample rate multiplier 000 = 1X 001 = 2X all others reserved
[27:26]	Rsvd	R	0x0	Reserved

Table 383. SPDIFIn VSR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[25:22]	OrigFS	R	0x0	Original sample rate (IEC spec).
[21:20]	CA	R	0x0	Clock accuracy 00 = Level II 01 = Level I 10 = Level III 11 = Reserved
[19:16]	FS	R	0x0	Sample Rate 0000 = 44.1 KHz 0010 = 48 KHz 0011 = 32 KHz All other combinations are reserved and shall not be used until further defined (IEC spec).
[15:12]	CN	R	0x0	Channel Number (audio channel) 0000 = do not take into account 0001 = A (left channel for stereo channel format) 0010 = B (right channel for stereo channel format) 0011 = C ... 1111 = O
[11:9]	WordLen	R	0x0	Sample Word Length [2:0] *If MaxWordLen = 1:* 000 = unspecified 001 = 20 bits 010 = 22 bits 011 = reserved 100 = 23 bits 101 = 24 bits 110 = 21 bits 111 = reserved *If MaxWordLen = 0:* 000 = unspecified 001 = 16 bits 010 = 18 bits 011 = reserved 100 = 19 bits 101 = 20 bits 110 = 17 bits 111 = reserved

Table 383. SPDIFIn VSR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[8]	MaxWordLen	R	0x0	Max Word Length 0 = maximum audio sample word length is 20 bits 1 = maximum audio sample word length is 24 bits
[7]	IgnoreBlkSz	RW	0x0	0 = normal behavior 1 = disable block size checking for SPDIF_IN.
[6]	IgnoreV	RW	0x0	0 = Respond to SPDIF_IN Valid tag 1 = Ignore SPDIF_IN valid tag
[5]	AutoMuteDis	RW	0x0	0 = Auto mute when SPDIF stream marked non PCM 1 = Auto Mute disabled.
[4:3]	ParityLimit	RW	0x0	SPDIF_IN Parity Limit: Loss of DPLL Lock after 00 = 4 parity errors 01 = 3 parity errors 10 = 2 parity errors 11 = 1 parity errors NEW LOCATION -- was at Register 72h, Page 0, D13:12, moved as part of SPDIF In consolidation
[2]	Running	R	0x0	SPDIF IN Running 0 = no signal on pin 47 1 = signal on pin 47 NEW LOCATION -- was at Register 72h, Page 0, D2, moved as part of SPDIF In consolidation
[1]	ParityErr	RW	0x0	SPDIF_IN PARITY ERROR. Set to clear. Overlaps SIPERSTAT.
[0]	InvertCOPY	RW	0x0	Copyright invert bit.

3.4.26. DigOut Node (NID = 0x21)

3.4.26.1. DigOut WCap

Table 384. DigOut WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 385. DigOut WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex
[19:16]	Delay	R	0x0	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No support for swapping left and right channels
[10]	PwrPrsnt	R	0x0	No support for Power State control
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x1	Connection list is present
[7]	UnsolCap	R	0x0	No support for Unsolicited Response
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.26.2. DigOut PinCap

Table 386. DigOut PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 387. DigOut PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x0	This widget does not control EAPD pin
[15:8]	VrefCap	R	0x00	Vref generation not supported on this pin
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x0	Pin complex is not input capable.
[4]	OutCap	R	0x1	Pin complex is output capable.
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.
[2]	PresDtctCap	R	0x0	Pin complex cannot perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

3.4.26.3. DigOut ConnSelect

Table 388. DigOut ConnSelect Command Verb Format

	Verb ID	Payload	Response
Get	F01	00	See bitfield table.
Set1	701	See bits [7:0] of bitfield table.	0000_0000h

Table 389. DigOut ConnSelect Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd	R	0x0	Reserved
[1:0]	Index	RW	0x0	Connection select control index.

3.4.26.4. DigOut ConnLen

Table 390. DigOut ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 391. DigOut ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x03	Number of NID entries in connection list.

3.4.26.5. DigOut ConnLst

Table 392. DigOut ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 393. DigOut ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x00	No connection
[23:16]	Entry2	R	0x1E	ADC1Mux widget
[15:8]	Entry1	R	0x1D	ADC0Mux widget
[7:0]	Entry0	R	0x1F	SPDIF Out Converter widget

3.4.26.6. DigOut PinCtl

Table 394. DigOut PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 395. DigOut PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:7]	Rsvd2	R	0x0	Reserved
[6]	OutEn	RW	0x0	1 = (CODEC) output path of Pin Widget is enabled
[5:0]	Rsvd1	R	0x0	Reserved

3.4.26.7. DigOut PinConfig

Table 396. DigOut PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 397. DigOut PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x0	External Port Connectivity of the Pin Complex. 0 = connected to a jack
[29:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23:20]	Device	RW	0x4	Default Device, indicating intended use of jack. 4 = SPDIF Out

Table 397. DigOut PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[19:16]	Connection	RW	0x4	Connection Type. 4 = RCA
[15:12]	Color	RW	0x2	Color of physical jack. 2 = Grey
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0x7	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.27. DigIn Node (NID = 0x22)

3.4.27.1. DigIn WCap

Table 398. DigIn WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 399. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x4	Widget type = Pin Complex. Pin Complex (4h) if SPDIFIn enabled, Vendor Defined (Fh) otherwise
[19:16]	Delay	R	0x3	Number of sample delays through widget
[15:12]	Rsvd1	R	0x0	Reserved
[11]	SwapCap	R	0x0	No left/right channel swap capability
[10]	PwrPrsnt	R	0x1	Power State control capability for support of EAPD
[9]	DigitalStrm	R	0x1	Widget supports a Digital stream
[8]	ConnList	R	0x0	No connection list is present

Table 399. DigIn WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7]	UnsolCap	R	0x1	Unsolicited Response is supported
[6]	ProcPrsnt	R	0x0	No Processing Controls parameter
[5]	Stripe	R	0x0	No support for striping
[4]	FrmtOverride	R	0x0	N/A for pin complex
[3]	AmpOverride	R	0x0	No amplifier info; use default amplifier parameters from Audio Function node instead
[2]	OutAmpPrsnt	R	0x0	No output amplifier
[1]	InAmpPrsnt	R	0x0	No input amplifier
[0]	Stereo	R	0x1	Stereo widget

3.4.27.2. DigIn PinCap

Table 400. DigIn PinCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0C	See bitfield table.

Table 401. DigIn PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd2	R	0x0	Reserved
[16]	EapdCap	R	0x1	This widget controls EAPD pin
[15:8]	VrefCap	R	0x00	Vref generation not supported on input pins.
[7]	Rsvd1	R	0x0	Reserved
[6]	BalancedIO	R	0x0	Pin complex does not have balanced pins.
[5]	InCap	R	0x1	Pin complex is input capable.
[4]	OutCap	R	0x0	Pin complex is not output capable. (EAPD = output stream)
[3]	HdphCap	R	0x0	Pin does not have a headphone amplifier.

Table 401. DigIn PinCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[2]	PresDtctCap	R	0x1	Pin complex can perform Presence Detect.
[1]	TrigRqd	R	0x0	N/A
[0]	ImpSenseCap	R	0x0	Pin complex does not support impedance sense.

3.4.27.3. DigIn PwrState

Table 402. DigIn PwrState Command Verb Format

	Verb ID	Payload	Response
Get	F05	00	See bitfield table.
Set1	705	See bits [7:0] of bitfield table.	0000_0000h

Table 403. DigIn PwrState Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7:4]	Act	R	0x3	PS-Act: Actual power state of referenced node.
[3:2]	Rsvd1	R	0x0	Reserved
[1:0]	Set	RW	0x3	PS-Set: Current power setting of referenced node. 00 - Fully on. 01 - Fully on. 10 - EAPD powered down (Hi-Z). 11 - Powered down (default)

3.4.27.4. DigIn PinCtl

Table 404. DigIn PinCtl Command Verb Format

	Verb ID	Payload	Response
Get	F07	00	See bitfield table.
Set1	707	See bits [7:0] of bitfield table.	0000_0000h

Table 405. DigIn PinCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:6]	Rsvd2	R	0x0	Reserved
[5]	InEn	RW	0x0	1 = (CODEC) input path of Pin Widget is enabled
[4:0]	Rsvd1	R	0x0	Reserved

3.4.27.5. DigIn UnsolResp

Table 406. DigIn UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 407. DigIn UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon lock or loss-of-lock of SPDIF_IN clock recovery circuit. Note that the DigEn field of SPDIFIn DigCtl must be set for the functionality to work.
[6]	Rsvd1	R	0x0	Reserved.
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.27.6. DigIn PinSense

Table 408. DigIn PinSense Command Verb Format

	Verb ID	Payload	Response
Get	F09	00	See bitfield table.
Set1	709	See bits [7:0] of bitfield table.	0000_0000h

Table 409. DigIn PinSense Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	PresDtct	R	0x0	For this widget, Presence Detect indicates that the SPDIF_IN clock recovery circuit has locked onto a valid SPDIF_IN sampling frequency. Any change in status will generate an Unsolicited Response, if enabled with verb 708. The SPDIF_IN clock recovery circuit must also be enabled (by setting SPDIFInDigCtl:DigEn).
[30:0]	Rsvd	R	0x0	Reserved. Impedance sense not supported for this Pin Complex.

3.4.27.7. DigIn EAPD

Table 410. DigIn EAPD Command Verb Format

	Verb ID	Payload	Response
Get	F0C	00	See bitfield table.
Set1	70C	See bits [7:0] of bitfield table.	0000_0000h

Table 411. DigIn EAPD Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:2]	Rsvd2	R	0x0	Reserved
[1]	Data	RW	0x0	EAPD value reflected on the EAPD pin. 0 = power down external amplifier; 1 = power up external amplifier if PwrState < 0x2. If PwrState > = 0x2, Pin47 is Hi-Z. An external pull-down is required if EAPD must be low when Pin Widget is powered down.
[0]	Rsvd1	R	0x0	Reserved

3.4.27.8. DigIn PinConfig

Table 412. DigIn PinConfig Command Verb Format

	Verb ID	Payload	Response
Get	F1C	00	See bitfield table.
Set1	71C	See bits [7:0] of bitfield table.	0000_0000h
Set2	71D	See bits [7:0] of bitfield table.	0000_0000h
Set3	71E	See bits [7:0] of bitfield table.	0000_0000h
Set4	71F	See bits [7:0] of bitfield table.	0000_0000h

Table 413. DigIn PinConfig Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:30]	Port	RW	0x1	External Port Connectivity of the Pin Complex. 1 = no physical connection
[29:24]	Location	RW	0x01	Physical location of the jack. 01h = Mainboard, Rear
[23:20]	Device	RW	0xC	Default Device, indicating intended use of jack. C = SPDIF In
[19:16]	Connection	RW	0x4	Connection Type. 4 = RCA
[15:12]	Color	RW	0x0	Color of physical jack. 0 = Unknown
[11:8]	Misc	RW	0x0	Misc[0] = Jack Detect override.
[7:4]	Assoc	RW	0xF	Default Association for Pin Complex groups. Reserved value 0000b should not be used. Value 1111b indicates lowest priority.
[3:0]	Sequence	RW	0x0	All Widgets in an association must have unique sequence number.

3.4.28. PCBeep Node (NID = 0x23)

3.4.28.1. PCBeep WCap

Table 414. PCBeep WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 415. PCBeep WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x7	Widget type = Beep Generator
[19:4]	Rsvd1	R	0x0	Reserved
[3]	AmpOverride	R	0x1	This widget contains its own amplifier parameters.
[2]	OutAmpPrsnt	R	0x1	Output amplifier is present
[1]	InAmpPrsnt	R	0x0	N/A
[0]	Stereo	R	0x0	Mono widget

3.4.28.2. PCBeep OutAmpCap

Table 416. PCBeep OutAmpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	12	See bitfield table.

Table 417. PCBeep OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31]	Mute	R	0x0	Amplifier is capable of muting
[30:23]	Rsvd3	R	0x0	Reserved
[22:16]	StepSize	R	0x17	Size of each step in the gain range = 6 dB
[15]	Rsvd2	R	0x0	Reserved

Table 417. PCBeep OutAmpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[14:8]	NumSteps	R	0x03	Number of steps in the gain range = 4 (-18dB to 0dB)
[7]	Rsvd1	R	0x0	Reserved
[6:0]	Offset	R	0x03	0dB-step is programmed with this offset

3.4.28.3. PCBeep Vol

Table 418. PCBeep Vol Command Verb Format

	Verb ID	Payload	Response
Get	BA0	00	See bitfield table.
Set1	3A0	See bits [7:0] of bitfield table.	0000_0000h

Table 419. PCBeep Vol Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x0	Reserved
[7]	Mute	RW	0x0	1 = disable Digital PC Beep
[6:2]	Rsvd1	R	0x0	Reserved
[1:0]	Gain	RW	0x0	Mono (left) amplifier gain step number

3.4.28.4. PCBeep Gen

Table 420. PCBeep Gen Command Verb Format

	Verb ID	Payload	Response
Get	F0A	00	See bitfield table.
Set1	70A	See bits [7:0] of bitfield table.	0000_0000h

Table 421. PCBeep Gen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7:0]	Divider	RW	0x0	Enable internal PC-Beep generation. Divider = 00h - disables internal PC Beep generation and enables normal operation of the CODEC. Divider not equal to 00h - generates the beep tone on all Pin Complexes that are currently configured as outputs. The HD Audio spec states that: beep tone frequency = (48 KHz HD Audio SYNC rate) / (4*Divider), producing tones from 47 Hz to 12 KHz (logarithmic scale). Instead, this part generates tones with frequency = 48000 * (257 - Divider) / 1024, yielding a linear range from 12 KHz to 93.75 Hz in steps of 46.875 Hz. If JackSenseVSR[Rate2x], then the beep tones generated have frequency = 48000 * (513 - Divider) / 1024, yielding a range of 24 KHz to 12093.75 Hz in steps of 46.875 Hz.

3.4.29. ExtVolume Node (NID = 0x24)

3.4.29.1. ExtVolume WCap

Table 422. ExtVolume WCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	09	See bitfield table.

Table 423. ExtVolume WCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:20]	Type	R	0x6	Widget type = Volume Knob Widget. Volume Knob (6h) if VOLUME enabled, Vendor Defined (Fh) otherwise
[19:0]	Rsvd1	R	0x0	Reserved. Software assumes capability of unsolicited responses and a connection list for this widget type.

3.4.29.2. ExtVolume KnobCap

Table 424. ExtVolume KnobCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	13	See bitfield table.

Table 425. ExtVolume KnobCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Delta	R	0x1	Indicates if software can write a base volume to the Volume Control Knob.
[6:0]	NumSteps	R	0x7F	Total number of steps in the range of the volume knob = 128

3.4.29.3. ExtVolume ConnLen

Table 426. ExtVolume ConnLen Command Verb Format

	Verb ID	Payload	Response
Get	F00	0E	See bitfield table.

Table 427. ExtVolume ConnLen Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved.
[7]	LongForm	R	0x0	Connection list uses short-form (7-bit) NID entries.
[6:0]	N	R	0x02	Number of NID entries in connection list. N = 02h if DAC1 enabled, N = 01h otherwise

3.4.29.4. ExtVolume ConnLst

Table 428. ExtVolume ConnLst Command Verb Format

	Verb ID	Payload	Response
Get	F02	00	See bitfield table.

Table 429. ExtVolume ConnLst Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Entry3	R	0x0	No connection.
[23:16]	Entry2	R	0x0	No connection.
[15:8]	Entry1	R	0x11	DAC1. Entry1 = 11h if DAC1 enabled, Entry1 = 00h otherwise
[7:0]	Entry0	R	0x10	DAC0

3.4.29.5. ExtVolume UnsolResp

Table 430. ExtVolume UnsolResp Command Verb Format

	Verb ID	Payload	Response
Get	F08	00	See bitfield table.
Set1	708	See bits [7:0] of bitfield table.	0000_0000h

Table 431. ExtVolume UnsolResp Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd2	R	0x00	Reserved
[7]	En	RW	0x0	Allow generation of Unsolicited Responses. Unsolicited response events occur upon jack-insertion OR completion of a Jack-Sense cycle.
[6]	Rsvd1	R	0x0	Reserved
[5:0]	Tag	RW	0x00	Software programmable field returned in top six bits (31:26) of every Unsolicited Response generated by this node.

3.4.29.6. ExtVolume KnobCtl

Table 432. ExtVolume KnobCtl Command Verb Format

	Verb ID	Payload	Response
Get	F0F	00	See bitfield table.
Set1	70F	See bits [7:0] of bitfield table.	0000_0000h

Table 433. ExtVolume KnobCtl Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:8]	Rsvd	R	0x0	Reserved
[7]	Direct	RW	0x0	Direct = 1 causes the volume control to directly control the hardware volume of the slave amps. Direct = 0 causes unsolicited responses to be generated.
[6:0]	Volume	RW	0x7F	Volume, specified in steps of amplifier gain

3.4.29.7. ExtVolume KnobVSR

Table 434. ExtVolume KnobVSR Command Verb Format

	Verb ID	Payload	Response
Get	FE0	00	See bitfield table.
Set1	7E0	See bits [7:0] of bitfield table.	0000_0000h

Table 435. ExtVolume KnobVSR Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:4]	Rsvd	R	0x0	Reserved
[3]	Continuous	RW	0x1	Allow continuous incrementing/decrementing of the volume knob value.
[2:0]	Rate	RW	0x0	Volume knob update rate, for continuous mode and de-bouncing (2.5 Hz to 20 Hz, in increments of 2.5 Hz)

4. ORDERING INFORMATION

Dolby Home Theater (HT) and Dolby Sound Room (SR) require the 5 V version of this part. Dolby Digital Live (DDL) characteristics are available in the 3.3 V version. Dolby also requires a separate license from Dolby to use their parts. IDT will only provide Dolby parts to Dolby approved customers.

TnR indicates availability on Tape and Reel. The minimum order quantity for TnR is 2,000 units.

Part Number	Voltage	Package	DAC	ADC	Modem	Digital Mics	Dolby	TnR
STAC9204D3TAEyyX	3.3 V	48 pin LQFP	4 channel	4 channel	No	No	Yes - DDL	No
STAC9204D3TAEyyXR	3.3 V	48 pin LQFP	4 channel	4 channel	No	No	Yes - DDL	Yes
STAC9204D5TAEyyX	5 V	48 pin LQFP	4 channel	4 channel	No	No	Yes - HT / SR	No
STAC9204D5TAEyyXR	5 V	48 pin LQFP	4 channel	4 channel	No	No	Yes - HT / SR	Yes
STAC9204X3TAEyyX	3.3 V	48 pin LQFP	4 channel	4 channel	No	No	No	No
STAC9204X3TAEyyXR	3.3 V	48 pin LQFP	4 channel	4 channel	No	No	No	Yes
STAC9204X5TAEyyX	5 V	48 pin LQFP	4 channel	4 channel	No	No	No	No
STAC9204X5TAEyyXR	5 V	48 pin LQFP	4 channel	4 channel	No	No	No	Yes
STAC9205D3TAEyyX	3.3 V	48 pin LQFP	4 channel	4 channel	No	Yes	Yes - DDL	No
STAC9205D3TAEyyXR	3.3 V	48 pin LQFP	4 channel	4 channel	No	Yes	Yes - DDL	Yes
STAC9205D5TAEyyX	5 V	48 pin LQFP	4 channel	4 channel	No	Yes	Yes - HT / SR	No
STAC9205D5TAEyyXR	5 V	48 pin LQFP	4 channel	4 channel	No	Yes	Yes - HT / SR	Yes
STAC9205X3TAEyyX	3.3 V	48 pin LQFP	4 channel	4 channel	No	Yes	No	No
STAC9205X3TAEyyXR	3.3 V	48 pin LQFP	4 channel	4 channel	No	Yes	No	Yes
STAC9205X5TAEyyX	5 V	48 pin LQFP	4 channel	4 channel	No	Yes	No	No
STAC9205X5TAEyyXR	5 V	48 pin LQFP	4 channel	4 channel	No	Yes	No	Yes
STAC9204D3NBEyyX	3.3 V	48 pad QFN	4 channel	4 channel	No	No	Yes - DDL	No
STAC9204D3NBEyyXR	3.3 V	48 pad QFN	4 channel	4 channel	No	No	Yes - DDL	Yes
STAC9204D5NBEyyX	5 V	48 pad QFN	4 channel	4 channel	No	No	Yes - HT / SR	No
STAC9204D5NBEyyXR	5 V	48 pad QFN	4 channel	4 channel	No	No	Yes - HT / SR	Yes
STAC9204X3NBEyyX	3.3 V	48 pad QFN	4 channel	4 channel	No	No	No	No
STAC9204X3NBEyyXR	3.3 V	48 pad QFN	4 channel	4 channel	No	No	No	Yes
STAC9204X5NBEyyX	5 V	48 pad QFN	4 channel	4 channel	No	No	No	No
STAC9204X5NBEyyXR	5 V	48 pad QFN	4 channel	4 channel	No	No	No	Yes
STAC9205D3NBEyyX	3.3 V	48 pad QFN	4 channel	4 channel	No	Yes	Yes - DDL	No
STAC9205D3NBEyyXR	3.3 V	48 pad QFN	4 channel	4 channel	No	Yes	Yes - DDL	Yes
STAC9205D5NBEyyX	5 V	48 pad QFN	4 channel	4 channel	No	Yes	Yes - HT / SR	No
STAC9205D5NBEyyXR	5 V	48 pad QFN	4 channel	4 channel	No	Yes	Yes - HT / SR	Yes
STAC9205X3NBEyyX	3.3 V	48 pad QFN	4 channel	4 channel	No	Yes	No	No
STAC9205X3NBEyyXR	3.3 V	48 pad QFN	4 channel	4 channel	No	Yes	No	Yes
STAC9205X5NBEyyX	5 V	48 pad QFN	4 channel	4 channel	No	Yes	No	No
STAC9205X5NBEyyXR	5 V	48 pad QFN	4 channel	4 channel	No	Yes	No	Yes

yy = CODEC revision number

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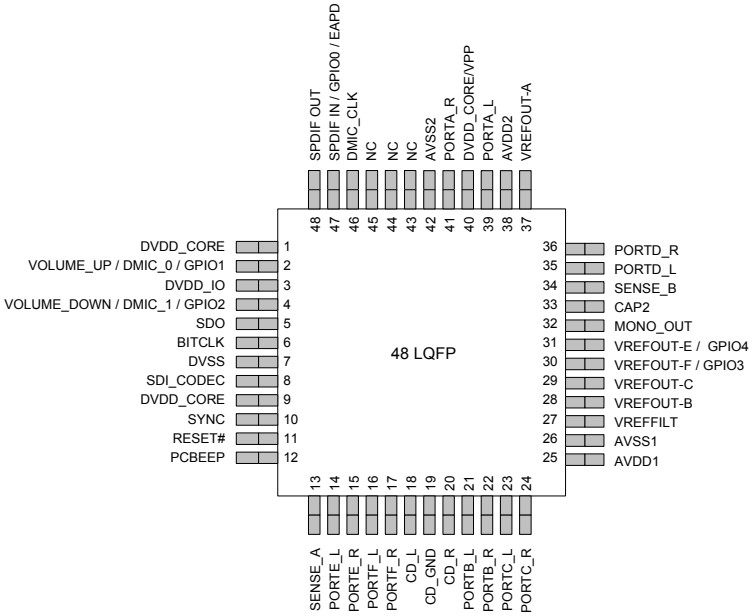
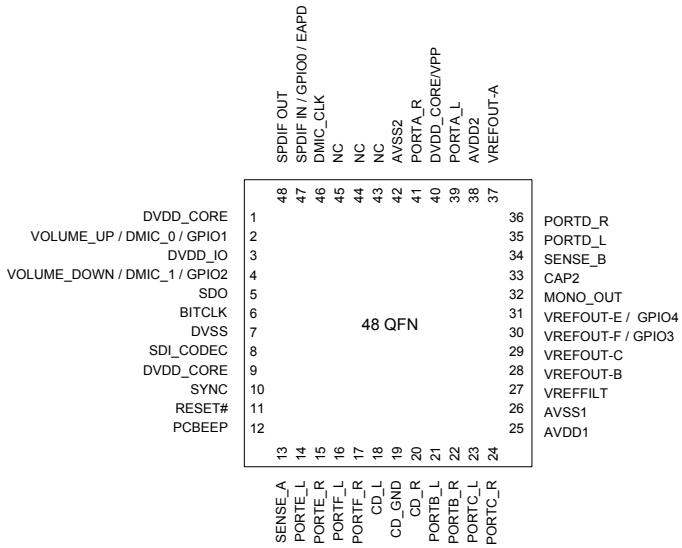
5. PINOUTS

5.1. Pin Assignment





5.2. Pin Descriptions

Pin No.	Pin Name	Pin Type	Internal Pull-up/ Pull-down	Pin Description
1	DVDD_CORE	I(Digital)	None	Digital Vdd = 3.3 V
2	Volume Up / DMIC0 / GPIO1	I/O(Digital)	50 KΩ pull-up with Volume or GPIO 50 KΩ pull-down with Digital Microphone	Volume Control or Digital Microphone 0 Input or General Purpose I/O
3	DVDD_IO	I(Digital)	None	Reference Voltage (1.5 V or 3.3 V)
4	Volume Down / DMIC1 / GPIO2	I/O(Digital)	50 KΩ pull-up with Volume or GPIO 50 KΩ pull-down with Digital Microphone	Volume Control or Digital Microphone 1 Input or General Purpose I/O
5	SDO	I/O(Digital)	None	HD Audio Serial Data output (inbound stream)
6	BITCLK	I(Digital)	None	HD Audio Bit Clock
7	DVSS	I(Digital)	None	Digital Ground
8	SDI_CODEC	O(Digital)	None	HD Audio Serial Data (outbound stream), audio module
9	DVDD_CORE	I(Digital)	None	Digital Vdd = 3.3 V

Pin No.	Pin Name	Pin Type	Internal Pull-up/ Pull-down	Pin Description
10	SYNC	I(Digital)	None	HD Audio Frame Sync
11	RESET#	I(Digital)	None	HD Audio Reset
12	PCBEEP	I(Analog)	None	PC Beep
13	SENSE_A	I(Analog)	None	Jack insertion detection Ports A, B, C, D
14	PORTE_L	I/O(Analog)	None	Input/Output of Left DAC0
15	PORTE_R	I/O(Analog)	None	Input/Output of Right DAC0
16	PORTF_L	I/O(Analog)	None	Input/Output of Left DAC1
17	PORTF_R	I/O(Analog)	None	Input/Output of Right DAC1
18	CD-L	I(Analog)	None	CD Audio Left Channel
19	CD-GND	I(Analog)	None	CD Audio Analog Ground
20	CD-R	I(Analog)	None	CD Audio Right Channel
21	PORTB_L	I/O(Analog)	None	Input/Output of Left DAC0 & DAC1
22	PORTB_R	I/O(Analog)	None	Input/Output of Right DAC0 & DAC1
23	PORTC_L	I/O(Analog)	None	Input/Output of Left DAC1
24	PORTC_R	I/O(Analog)	None	Input/Output of Right DAC1
25	AVDD1	I(Analog)	None	Analog Vdd = 5.0 V or 3.3 V
26	AVSS1	I(Analog)	None	Analog Ground
27	VREFFILT	O(Analog)	None	Analog Virtual Ground
28	VREFOUT-B	O(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port B
29	VREFOUT-C	O(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port C
30	VREFOUT-F / GPIO3	IO(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port F or analog GPIO3
31	VREFOUT-E / GPIO4	IO(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port E or analog GPIO4
32	MONO_OUT	O(Analog)	None	Mono output of DAC0
33	CAP2	O(Analog)	None	ADC reference Capacitor
34	SENSE_B	I(Analog)	None	Jack insertion detection Ports E, F
35	PORT-D_L (HP)	I/O(Analog)	None	Input/Output of Left DAC0
36	PORT-D_R (HP)	I/O(Analog)	None	Input/Output of Right DAC0

Pin No.	Pin Name	Pin Type	Internal Pull-up/ Pull-down	Pin Description
37	VREFOUT-A	O(Analog)	None	Reference Voltage out drive (intended for microphone bias) for Port A
38	AVDD2	I(Analog)	None	Analog Vdd = 5.0 V or 3.3 V
39	PORTA_L (HP)	I/O(Analog)	None	Input/Output of Left DAC0 & 1
40	DVDD_CORE	I(Analog)	None	DVDD
41	PORTA_R (HP)	I/O(Analog)	None	Input/Output of Right DAC0 & 1
42	AVSS2	I(Analog)	None	Analog Ground
43	NC	None	None	No Connect
44	NC	None	None	No Connect
45	NC	None	None	No Connect
46	DMIC_CLK	O(Digital)	50 KΩ pull-down	Digital Microphone Output Clock
47	SPDIFIN / GPIO0 / EAPD	I/O(Digital)	50 KΩ pull-up	SPDIF Input, General Purpose I/O, EAPD
48	SPDIF-OUT	O(Digital)	Internal 50 KΩ pull-down	SPDIF digital output

6. DESIGN CONSIDERATIONS

6.1. External Components

The STAC9204/9205 requires a minimum number of external components for proper operation.

6.1.1. Decoupling Capacitor

Decoupling capacitors must be connected between AVDD and AVSS and between DVDD and DVSS, as close to these pins as possible.

- Between AVDD (pin 38) and AVSS (pins 26 and 42), use a 1.0 mF capacitor in parallel with a 10 mF capacitor.
- Between AVDD (pin 25) and AVSS (pins 26 and 42), use a 0.1 mF capacitor in parallel with a 10 mF capacitor.
- Between DVDD (pin 1) and DVSS (pins 4 and 7), use a 1.0 mF capacitor in parallel with a 10 mF capacitor.
- Between DVDD (pin 9) and DVSS (pins 4 and 7), use a 0.1 mF capacitor in parallel with a 10 mF capacitor.

For optimum device performance, the decoupling capacitors should be mounted on the CODEC side of the PCB. Avoid the use of vias in the decoupling circuit.

6.1.2. Other Required Components

The following components are required:

- Between VREFFILT (pin 27) and AVSS (pins 26 and 42), use a 1.0 mF capacitor in parallel with a 10 mF capacitor.
- Each of these pins needs to have an 820 pF capacitor connected to AVSS (pins 26 and 42). (Recommend using NP0 type capacitor.)
  - ADC0_AFILT_L (pin 28).
  - ADC1_AFILT_L (pin 29).
  - ADC0_AFILT_R (pin 30).
  - ADC1_AFILT_R (pin 31).
- ADC_VREF (pin 33) must have a 1.0 mF capacitor connected to AVSS (pins 26 and 42). Optionally, a 10 mF capacitor may also be connected in parallel, to improve performance.
- SENSE_A (pin 13) and SENSE_B (pin 34) must each be connected to AVSS (pins 26 and 42) with a 1000 pF capacitor located as close to the pins as possible.
- SENSE_A (pin 13) and SENSE_B (pin 34) must each be connected to AVDD (pins 25 and 38) with a 5.11 KW resistor. This resistor MUST be 1% tolerance and should be located as close to the pins as possible.
- Either SENSE_A or SENSE_B is connected to each Port through a resistor. This resistor MUST be 1% or better tolerance. (For resistor details, see Table 3. For details about these connections, see the latest IDT reference designs.)

For optimum device performance, these components should be mounted on the CODEC side of the PCB. Minimize the use of vias.

6.2. PCB Layout Recommendations

An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the STAC9204/9205. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Separate analog and digital grounding is recommended. The analog grounds (AVSS (pins 26 and 42)) and the digital grounds (DVSS (pins 4 and 7)) should be tied together at only one place. This tie should be under the CODEC.

Capacitive coupling is allowed for EMI considerations. Generally, use 0.1 mF capacitors. Make sure these are spread out in the layout.

Analog ground (AVSS) should be located on all grounding layers. AVSS should be the same shape on these layers.

Analog audio signals should not escape the AVSS cut.

Analog non-audio signals should not enter the AVSS cut.

Only audio voltage planes (such as AVDD) should be located on the VCC layer.

Analog voltage should be provided from a filtered source. LDO's are preferred. Ferrite beads are acceptable. Whichever is used must support current requirements.

6.2.1. Vista WLP Compliance Requirements

The following external components are REQUIRED for Vista WLP compliance.

Required series coupling capacitors on analog I/O signal lines:

- Minimum Premium Desktop Implementations:
  - Line Output = 10 mF, 1206, 10 V, X5R (ceramic) or 3.3 mF aluminum electrolytic (or similar).
  - Headphone Output = 220 mF aluminum electrolytic (or similar).
  - Microphone or Line Input = 1 mF, 0603, X5R (ceramic) or better.
- Minimum Premium Mobile Implementations:
  - Line Output = 2.2 mF, 1206, 16 V, X5R (ceramic).
  - Headphone Output = 100 mF D-Case size (or similar). Larger is better, we usually recommend 220 mF.
  - Microphone or Line Input = 1 mF, 0603, X5R (ceramic) or better.

EMI Components:

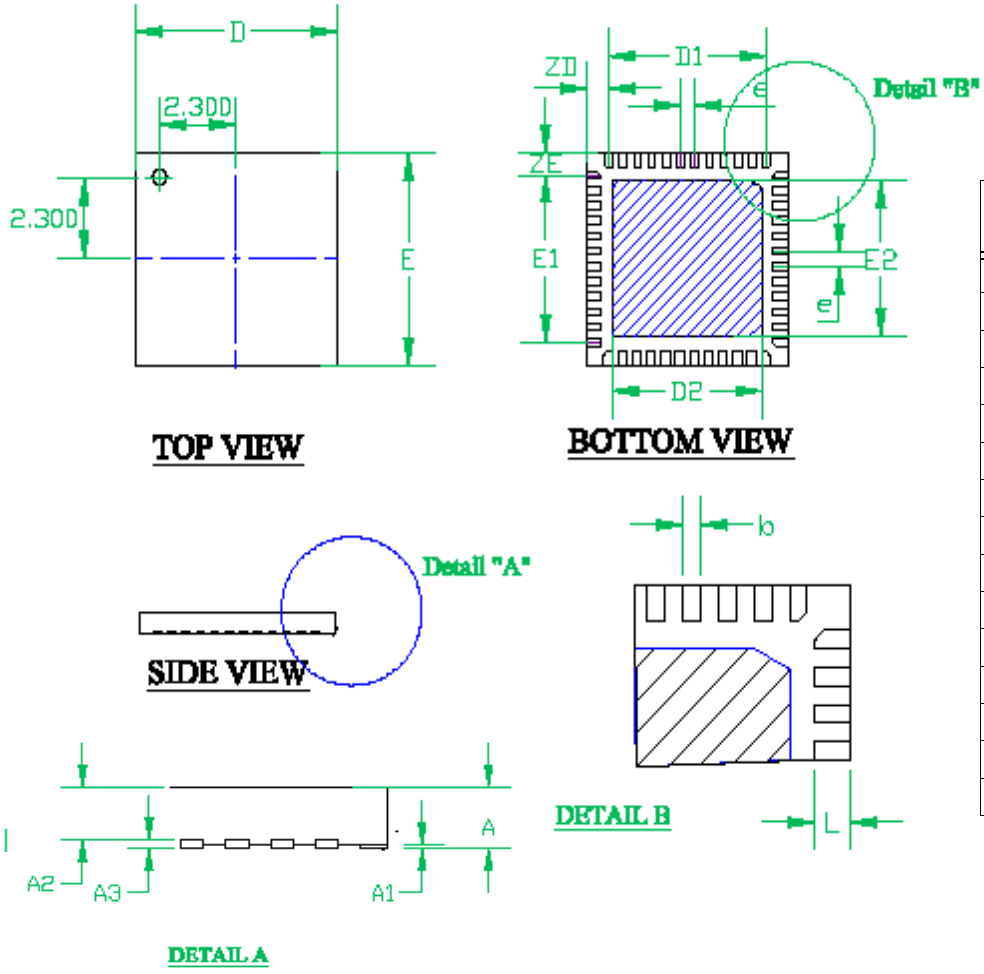
- Recommended Ferrite Beads are 600 ohm. Use these manufacturers only:
  - TDK - MMZ1608Y601BTA
  - MURATA - BLM18BD601SN1
  - TAIYO YUDEN - LF BK 1608HM601-T
- EMI shunt capacitor:
  - For Headphone ports, 0.01 mF.
  - For all other ports, 100 pF.
  - EMI components should be placed as close to the jack as possible.

Note: See the latest STAC9204/9205/9204D/9205D Reference Designs for further details on schematic recommendations.

7. PACKAGE OUTLINE AND PACKAGE DIMENSIONS

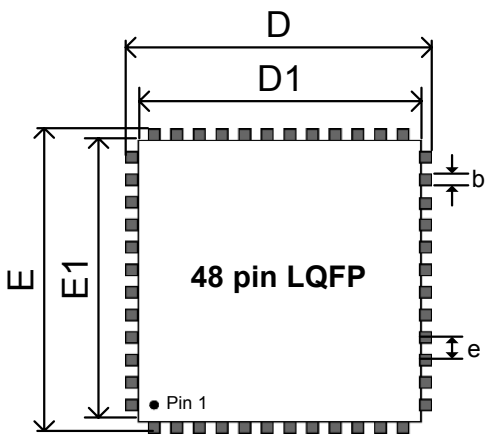
Package dimensions are kept current with JEDEC Publication No. 95

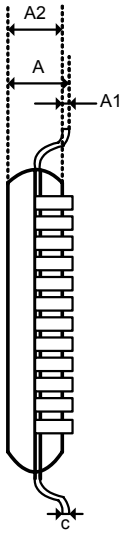
7.1. 48-Pad QFN Package



Key	QFN Dimensions in mm		
	Min	Nom	Max
A	0.80	0.90	1.0
A1	0.00	0.02	0.05
A3		0.20 REF	
D		7.00 BSC	
D1		5.50 BSC	
E		7.00 BSC	
E1		5.50 BSC	
L	0.35	0.40	0.45
e		0.50 BSC	
R		0.20-0.25	
b	0.18	0.25	0.30
D2	5.50	5.65	5.80
E2	5.50	5.65	5.80
ZD		0.75 BSC	
ZE		0.75 BSC	

7.2. 48-Pin LQFP Package





Key	LQFP Dimensions in mm		
	Min	Nom	Max
A	1.40	1.50	1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
e		0.50	
c	0.09	-	0.20
b	0.17	0.22	0.27

8. SOLDER REFLOW PROFILE

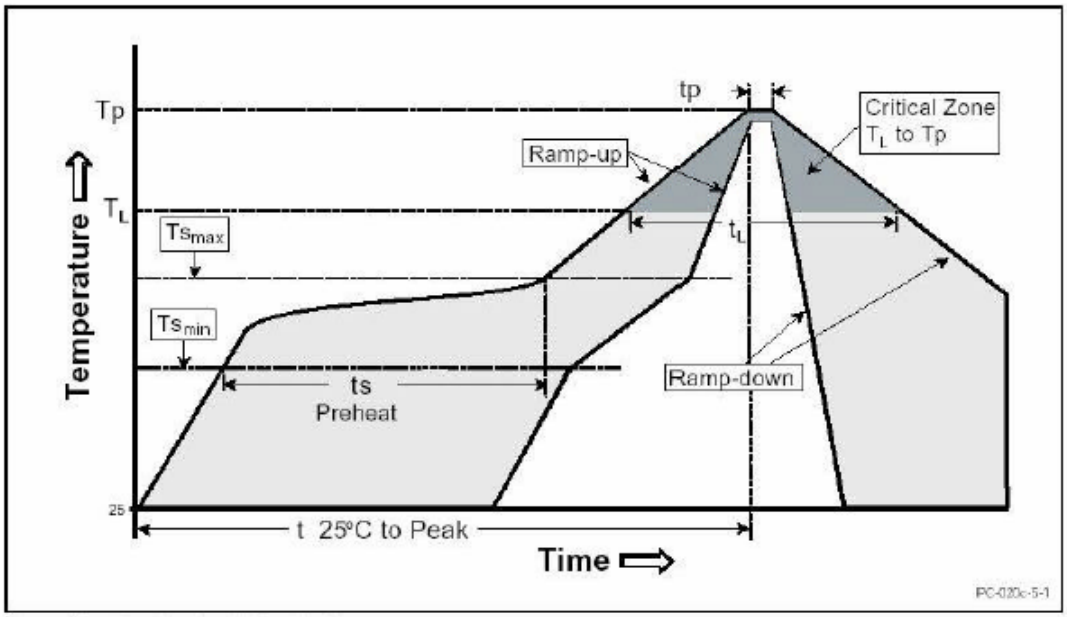
8.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices" (www.jedec.org/download).

Profile Feature		Pb Free Assembly
Average Ramp-Up Rate (Ts_{max} - Tp)		3 °C / second max
Preheat:	Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} - ts_{max})	150 °C 200 °C 60 - 180 seconds
Time maintained above:	Temperature (T_L) Time (t_L)	217 °C 60 - 150 seconds
Peak / Classification Temperature (Tp)		See "Package Classification Reflow Temperatures" on page 190.
Time within 5 °C of actual Peak Temperature (tp)		20 - 40 seconds
Ramp-Down rate		6 °C / second max
Time 25 °C to Peak Temperature		8 minutes max
Note: All temperatures refer to topside of the package, measured on the package body surface.		

Figure 7. Solder Reflow Profile



8.2. Pb Free Process - Package Classification Reflow Temperatures

Package Type	MSL	Reflow Temperature
LQFP 48-pin	3	260 ^{O}C
QFN 48-pad	3	260 ^{O}C

9. REVISION HISTORY

Revision	Date	Description of Change
0.8	22 September 2006	Initial release in IDT format.
0.81	9 November 2006	Updated to match IDT standard documents.
0.82	17 November 2006	Incorporated Widget list into section 3.
1.0	December 2006	Updated electrical characteristics based on validation data. Removed use of colored line in block and widget diagrams.

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www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
HA.CM@idt.com

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Europe
IDT Europe, Limited
Prime House
Barnett Wood Lane
Leatherhead, Surrey
United Kingdom KT22 7DE
+44 1372 363 339